EE692 Applied EM- FDTD Method
One-Dimensional Transmission Lines Notes- Lecture 4

FDTD Modeling of Voltage Sources and Terminations with Parallel/Series RLC Loads

As the final step toward modeling transmission line circuits (see Figure 1), this lecture will present the FDTD update equations necessary to implement voltage sources and transmission line terminations with parallel or series RLC loads in the one-dimensional (1-D) FDTD transmission line model [1]. This is an extension of the work to implement single lumped circuit elements (e.g., capacitors, inductors, and resistors) [2] and parallel or series RLC loads [3-4] placed in parallel or series with the transmission line presented in prior lectures. The work on single lumped elements can be adapted in a similar fashion. Some results will be shown to demonstrate the accuracy and validity of the update equations by comparison with analytic results.

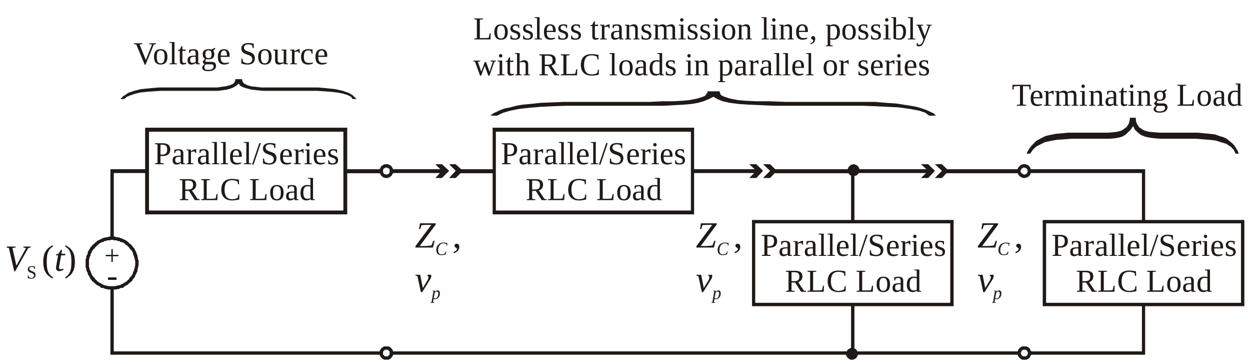

Figure 1 Transmission line circuit.

Voltage source with series RLC load in series

Figure 2 shows the circuit representation, incremental, and discretized incremental models for a voltage source with series RLC elements in series. In Figure 2, *l* is the inductance per unit length, and *c* is the capacitance per unit length, and *R*, *L*, and *C* are the lumped element resistor, inductor, and capacitor respectively.

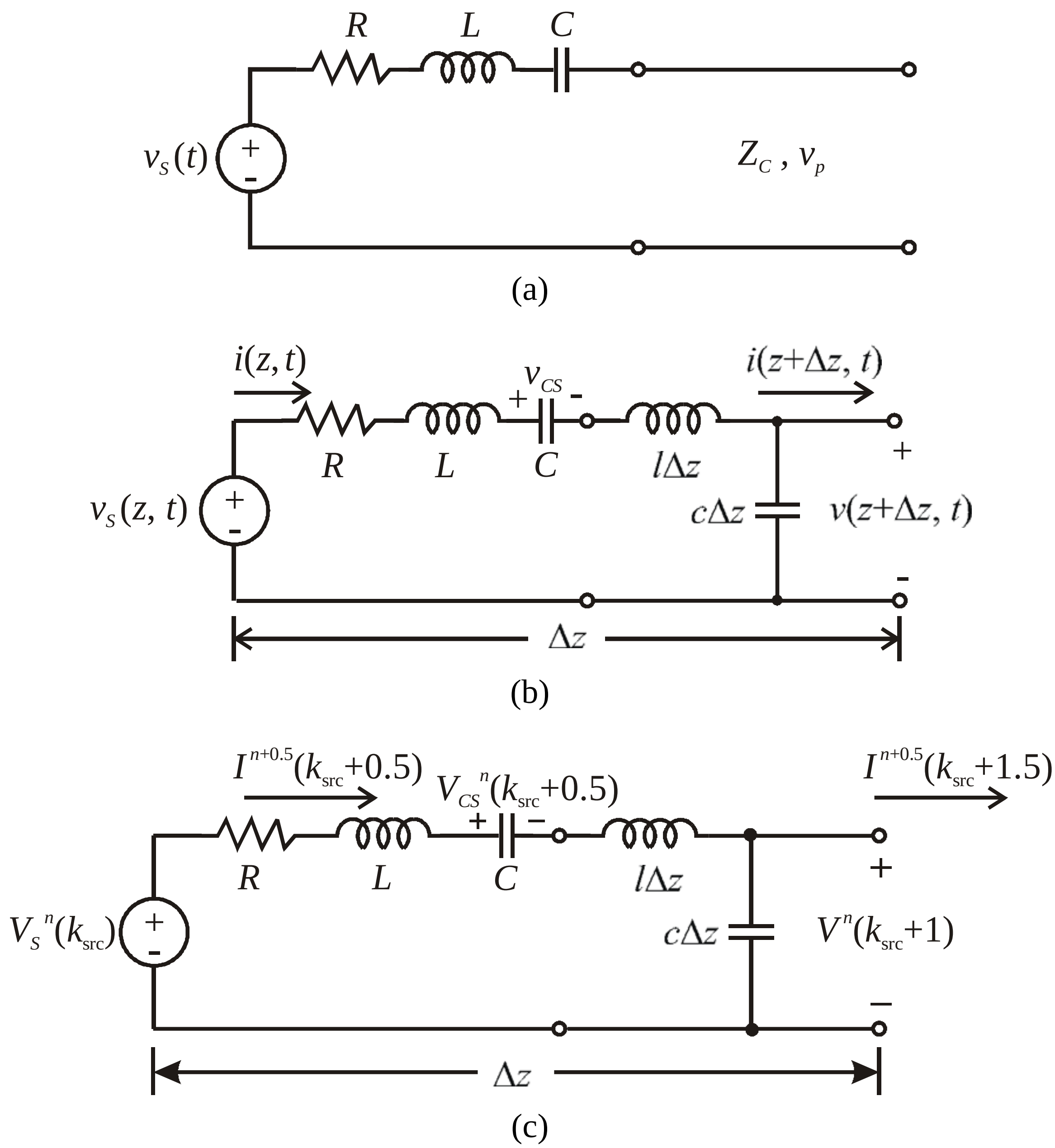

Figure 2 (a) Circuit representation, (b) incremental, and (c) discretized incremental models of a voltage source with lumped element series RLC load in series.

Applying Kirchoff's Current Law (KCL) to the top right node of Figure 2b yields

$$i(z,t) - i(z+\Delta z,t) - c\Delta z \frac{\partial v(z+\Delta z,t)}{\partial t} = 0 .$$

Applying Kirchoff's Voltage Law (KVL) clockwise around the outside loop of Figure 2b yields

$$v(z+\Delta z,t) - v_S(z,t) + R\, i(z,t) + L\frac{\partial i(z,t)}{\partial t} + v_{CS} + l\Delta z \frac{\partial i(z,t)}{\partial t} = 0$$

where

$$v_{CS}(z,t) = \frac{1}{C}\int_{t_0}^{t} i(z,t)\,\partial t + v_{CS}(z,t_0) .$$

These equations, when discretized (see RLC loads lecture material), re-arranged and simplified, yield the update equations

$$\boxed{V_{CS}{}^{n}(k_{\text{src}}+0.5) = V_{CS}{}^{n-1}(k_{\text{src}}+0.5) + \frac{\Delta t}{C} I^{n-0.5}(k_{\text{src}}+0.5)} ,$$

$$\boxed{\begin{aligned} I^{n+0.5}(k_{\text{src}}+0.5) = B_1 I^{n-0.5}(k_{\text{src}}+0.5) - B_2 \frac{1}{Z_C}\left(\frac{v_p \Delta t}{\Delta z}\right)\left[V^n(k_{\text{src}}+1) - V_S^n(k_{\text{src}})\right] \\ -B_2 \frac{1}{Z_C}\left(\frac{v_p \Delta t}{\Delta z}\right) V_{CS}{}^{n}(k_{\text{src}}+0.5) \end{aligned}} ,$$

and

$$\boxed{V^{n+1}(k_{\text{src}}+1) = V^n(k_{\text{src}}+1) - Z_C\left(\frac{v_p \Delta t}{\Delta z}\right)\left[I^{n+0.5}(k_{\text{src}}+1.5) - I^{n+0.5}(k_{\text{src}}+0.5)\right]}$$

where

$$\boxed{B_1 = \frac{1 - \frac{1}{Z_C}\left(\frac{v_p \Delta t}{\Delta z}\right)\left(\frac{R}{2} - \frac{L}{\Delta t}\right)}{1 + \frac{1}{Z_C}\left(\frac{v_p \Delta t}{\Delta z}\right)\left(\frac{R}{2} + \frac{L}{\Delta t}\right)}}$$

and

$$\boxed{B_2 = \frac{1}{1 + \frac{1}{Z_C}\left(\frac{v_p \Delta t}{\Delta z}\right)\left(\frac{R}{2} + \frac{L}{\Delta t}\right)}} .$$

Again, define the characteristic impedance $Z_C = \sqrt{\frac{l}{c}}$, phase velocity $v_p = \frac{1}{\sqrt{lc}}$, and Courant stability factor $S = \frac{v_p \Delta t}{\Delta z}$. This implies $l = \frac{Z_C}{v_p}$ and $c = \frac{1}{v_p Z_C}$. Note, there is an auxiliary equation to update the voltage across the series lumped capacitor V_{CS}. Further, the current update equation has several modifications (when compared to that for a 1D lossless transmission line) that account for the series RLC load in series- an additional term for V_{CS}, the left-hand voltage $V^n(k)$ has been replaced with the discretized source voltage $V_S^n(k_{\text{src}})$, and there are coefficients that account for the series lumped-element inductor and resistor in series. The update equation for the voltage is unchanged from that for a 1D lossless transmission line.

The series RLC load in series with the voltage source and the lossless 1D transmission line is located at $z = (k_{\text{src}} + 0.5)\Delta z$ in the FDTD grid. In the FDTD spatial grid, the voltage source is placed at location $z = k_{\text{src}} \Delta z$. In most instances $k_{\text{src}} = 0$ and $z = 0$ are selected (source at the beginning of the transmission line). This allows the update equations to begin with the current and voltage nodes at spatial indices of k = 1 which is well suited to most programming languages. Further, the voltage source is a “hard source”, i.e., $V_S^n(k_{\text{src}}) = v_S(n\Delta t)$, that is not effected by surrounding currents and voltages.

Voltage source with parallel RLC load in series

Figure 3 shows the circuit representation, incremental, and discretized incremental models for a voltage source with parallel RLC elements in series.

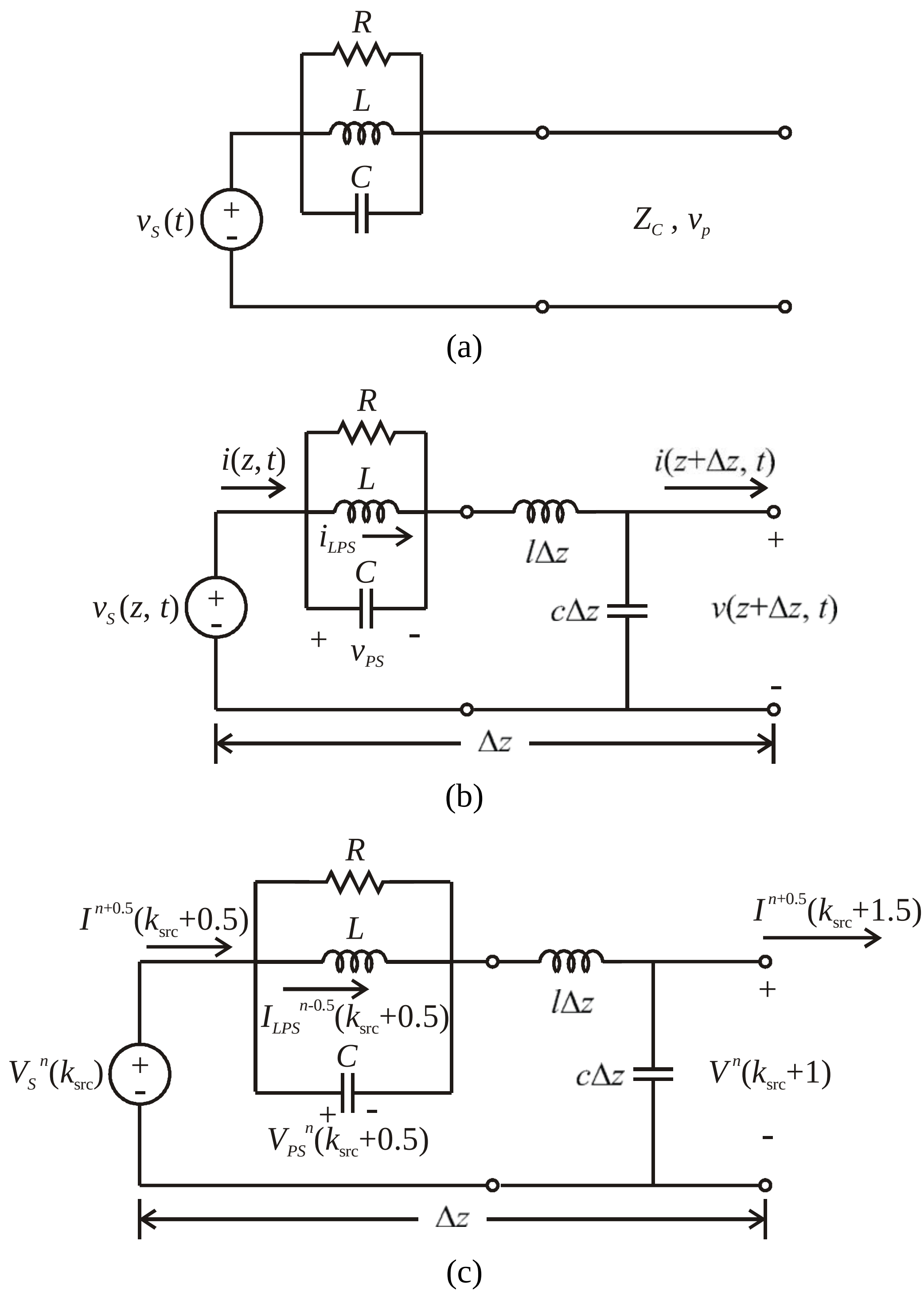

Figure 3 (a) Circuit representation, (b) incremental, and (c) discretized incremental models of a voltage source with lumped element parallel RLC load in series.

Applying KCL to the top right node of Figure 3b yields

$$i(z,t) - i(z+\Delta z,t) - c\Delta z \frac{\partial v(z+\Delta z,t)}{\partial t} = 0.$$

Applying KCL to the top left node of Figure 3b yields

$$i(z,t) - \frac{v_{PS}}{R} - i_{LPS} - C\frac{\partial v_{PS}}{\partial t} = 0$$

where

$$i_{LPS}(z,t) = \frac{1}{L}\int_{t_0}^{t} v_{PS}(z,t)\partial t + i_{LPS}(z,t_0).$$

Applying KVL clockwise around the outside loop of Figure 3b yields

$$v(z+\Delta z,t) - v_S(z,t) + v_{PS} + l\Delta z\frac{\partial i(z,t)}{\partial t} = 0.$$

These equations, when discretized (see RLC loads lecture material), re-arranged and simplified, yield the update equations

$$\boxed{I_{LPS}^{n-0.5}(k_{\text{src}}+0.5) = I_{LPS}^{n-1.5}(k_{\text{src}}+0.5) + \frac{\Delta t}{L}V_{PS}^{n-1}(k_{\text{src}}+0.5)},$$

$$\boxed{\begin{aligned} V_{PS}^{n}(k_{\text{src}}+0.5) &= \left[\frac{\frac{C}{\Delta t}-\frac{1}{2R}}{\frac{C}{\Delta t}+\frac{1}{2R}}\right]V_{PS}^{n-1}(k_{\text{src}}+0.5) \\ &+\left[\frac{1}{\frac{C}{\Delta t}+\frac{1}{2R}}\right]\left[I^{n-0.5}(k_{\text{src}}+0.5) - I_{LPS}^{n-0.5}(k_{\text{src}}+0.5)\right] \end{aligned}},$$

$$\boxed{\begin{aligned} I^{n+0.5}(k_{\text{src}}+0.5) &= I^{n-0.5}(k_{\text{src}}+0.5) - \frac{1}{Z_C}\left(\frac{v_p\Delta t}{\Delta z}\right)\left[V^{n}(k_{\text{src}}+1) - V_S^{n}(k_{\text{src}})\right] \\ &-\frac{1}{Z_C}\left(\frac{v_p\Delta t}{\Delta z}\right)V_{PS}^{n}(k_{\text{src}}+0.5) \end{aligned}},$$

and

$$\boxed{V^{n+1}(k_{\text{src}}+1) = V^{n}(k_{\text{src}}+1) - Z_C\left(\frac{v_p\Delta t}{\Delta z}\right)\left[I^{n+0.5}(k_{\text{src}}+1.5) - I^{n+0.5}(k_{\text{src}}+0.5)\right]}.$$

There are two auxiliary equations to update the voltage across the lumped element capacitor v_{PS} and current through the lumped element inductor i_{LPS}. Also, the current update equation has two modifications (when compared to that for a 1D lossless transmission line) that account for the parallel RLC load in series - an additional term for V_{PS} and the left-hand voltage $V^n(k)$ has been replaced with the discretized source voltage $V_S^n(k_{\text{src}})$. However, the update equation for the voltage is unchanged from that for a 1D lossless transmission line.

The parallel RLC load in series with the voltage source and the lossless 1D transmission line is located at $z=(k_{\text{src}}+0.5)\Delta z$ in the FDTD grid. In the FDTD spatial grid, the voltage source is placed at location $z=k_{\text{src}}\Delta z$. In most instances $k_{\text{src}}=0$ and $z=0$ are selected (source at the beginning of the transmission line). This allows the update equations to begin with the current and voltage nodes at spatial indices of k = 1 which is well suited to most programming languages. Further, the voltage source is a “hard source”, i.e., $V_S^n(k_{\text{src}})=v_S(n\Delta t)$, that is not effected by surrounding currents and voltages.

Series RLC transmission line termination

Figure 4 shows the circuit representation, incremental, and discretized incremental models for a lossless 1D transmission line terminated with series RLC elements.

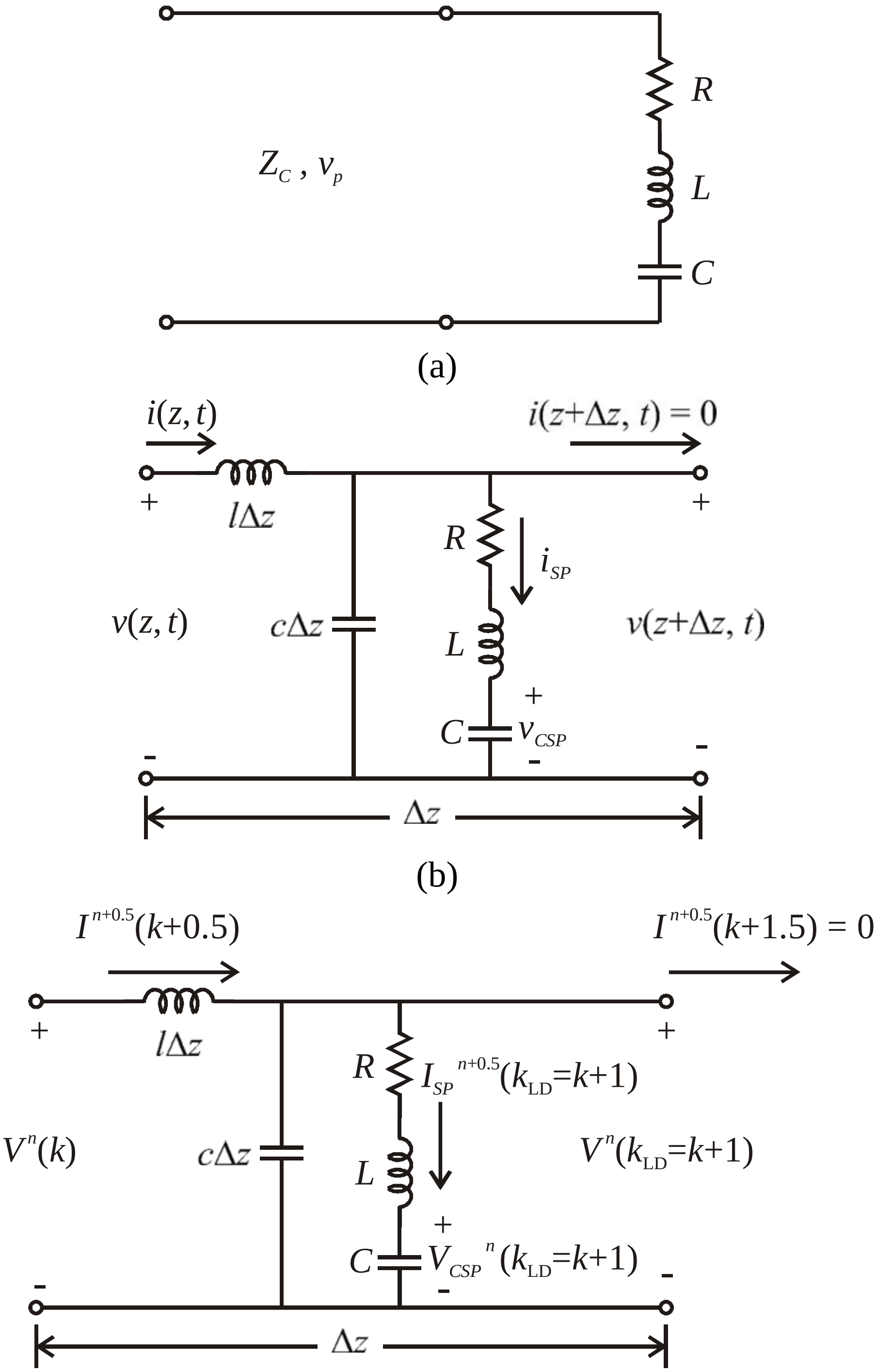

Figure 4 (a) Circuit representation, (b) incremental, and (c) discretized incremental models of a terminating lumped-element series RLC load.

Applying KCL to the top right node of Figure 4b (no current at $k + 1.5$) yields

$$i(z,t) - c\Delta z \frac{\partial v(z+\Delta z,t)}{\partial t} - i_{SP} = 0 .$$

Applying KVL clockwise around the outside loop of Figure 4b yields

$$v(z+\Delta z,t) - v(z,t) + l\Delta z \frac{\partial i(z,t)}{\partial t} = 0 .$$

Applying KVL counterclockwise around the right-hand loop of the circuit of Figure 4b yields

$$i_{SP} R + L\frac{\partial i_{SP}}{\partial t} + v_{CSP} - v(z+\Delta z,t) = 0$$

where

$$v_{CSP}(z+\Delta z,t) = \frac{1}{C}\int_{t_0}^{t} i_{SP}(z+\Delta z,t)\partial t + v_{CSP}(z+\Delta z,t_0) .$$

These equations, when discretized (see RLC loads lecture material), re-arranged and simplified, yield the update equations

$$\boxed{V_{CSP}{}^{n}(k+1) = V_{CSP}{}^{n-1}(k+1) + \frac{\Delta t}{C} I_{SP}^{n-0.5}(k+1)} ,$$

$$\boxed{I_{SP}{}^{n+0.5}(k+1) = \left[\frac{\frac{L}{\Delta t} - \frac{R}{2}}{\frac{L}{\Delta t} + \frac{R}{2}}\right] I_{SP}{}^{n-0.5}(k+1) + \left[\frac{1}{\frac{L}{\Delta t} + \frac{R}{2}}\right]\left[V^{n}(k+1) - V_{CSP}{}^{n}(k+1)\right]} ,$$

$$\boxed{I^{n+0.5}(k+0.5) = I^{n-0.5}(k+0.5) - \frac{1}{Z_c}\left(\frac{v_p \Delta t}{\Delta z}\right)\left[V^{n}(k+1) - V^{n}(k)\right]} ,$$

and

$$\boxed{V^{n+1}(k+1) = V^{n}(k+1) + Z_c\left(\frac{v_p \Delta t}{\Delta z}\right) I^{n+0.5}(k+0.5) - Z_c\left(\frac{v_p \Delta t}{\Delta z}\right) I_{SP}{}^{n+0.5}(k+1)} .$$

Note that the update equations contain two intermediate auxiliary variables- one for the current i_{SP} through the terminating series RLC load and one for the voltage across the lumped capacitor v_{CSP}. The voltage update equation has an additional term (when compared to that for a 1D lossless transmission line) that accounts for the terminating series RLC load, and is minus the right-hand current term. Also, the terminating series RLC load is located at $z = (k+1)\Delta z = k_{\mathrm{LD}}\Delta z$ in the FDTD grid.

Parallel RLC transmission line termination

Figure 5 shows the circuit representation, incremental, and discretized incremental models for a lossless 1D transmission line with a terminating parallel lumped element RLC load.

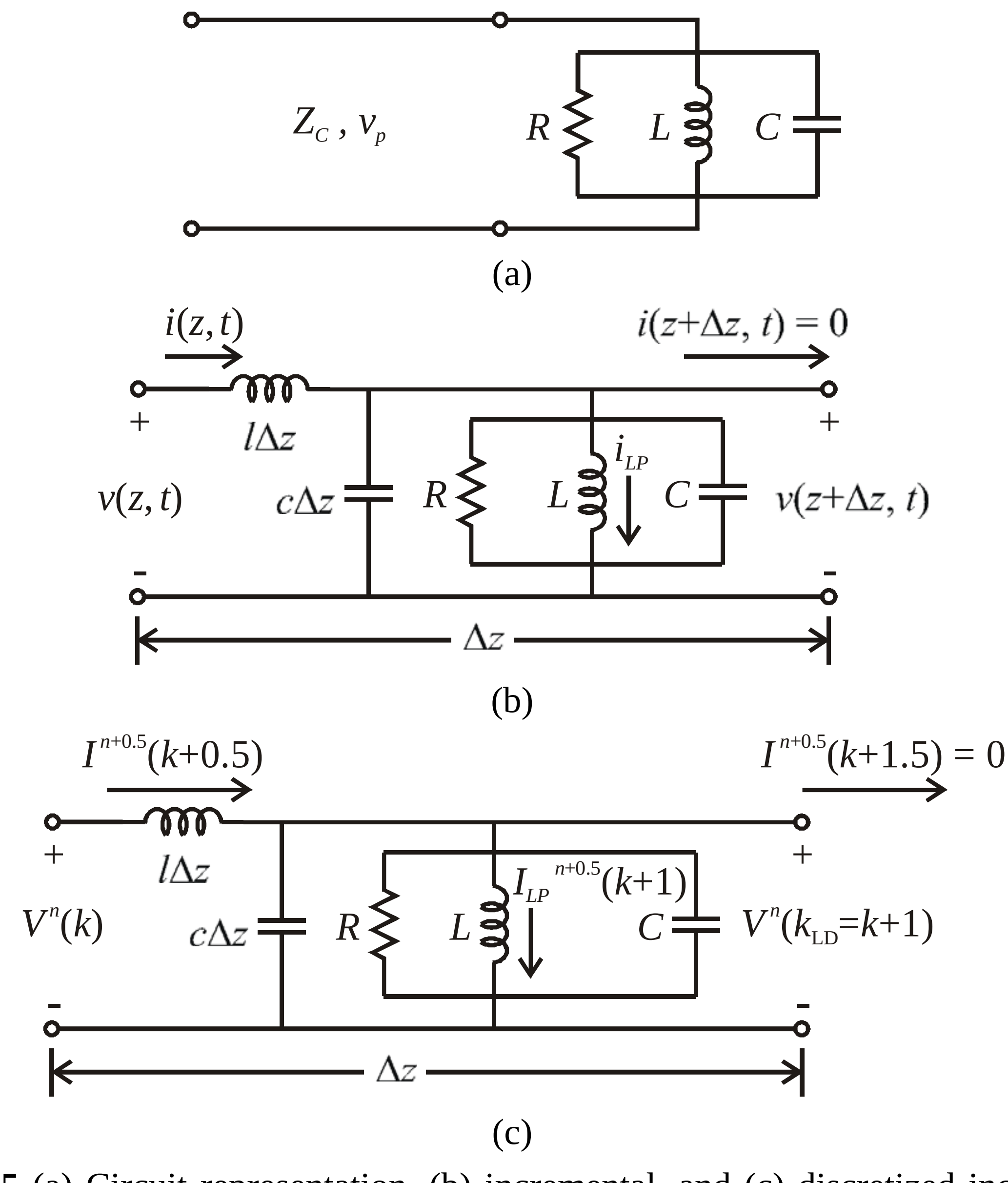

Figure 5 (a) Circuit representation, (b) incremental, and (c) discretized incremental models of a terminating lumped element parallel RLC load.

Applying Kirchoff's Current Law (KCL) to the top right node of Figure 5b yields

$$i(z,t) - c\Delta z \frac{\partial v(z+\Delta z,t)}{\partial t} - C\frac{\partial v(z+\Delta z,t)}{\partial t} - \frac{v(z+\Delta z,t)}{R} - i_{LP} = 0$$

where i_{LP} is defined by the integral equation

$$i_{LP}(z+\Delta z,t)=\frac{1}{L}\int_{t_0}^{t} v(z+\Delta z,t)\partial t + i_{LP}(z+\Delta z,t_0).$$

Applying Kirchoff's Voltage Law (KVL) clockwise around the outside loop of Figure 5b yields

$$v(z+\Delta z,t)-v(z,t)+l\Delta z\frac{\partial i(z,t)}{\partial t}=0.$$

These equations, when discretized (see RLC loads lecture material), re-arranged and simplified, yield the update equations

$$\boxed{I^{n+0.5}(k+0.5)=I^{n-0.5}(k+0.5)-\frac{1}{Z_C}\left(\frac{v_p\Delta t}{\Delta z}\right)\left[V^n(k+1)-V^n(k)\right]},$$

$$\boxed{I_{LP}^{n+0.5}(k+1)=I_{LP}^{n-0.5}(k+1)+\frac{\Delta t}{L}V^n(k+1)},$$

and

$$\boxed{V^{n+1}(k+1)=A_1V^n(k+1)+A_2Z_C\left(\frac{v_p\Delta t}{\Delta z}\right)I^{n+0.5}(k+0.5)-A_2Z_C\left(\frac{v_p\Delta t}{\Delta z}\right)I_{LP}{}^{n+0.5}(k+1)}$$

where

$$\boxed{A_1=\frac{1-Z_C\left(\frac{v_p\Delta t}{\Delta z}\right)\left(\frac{1}{2R}-\frac{C}{\Delta t}\right)}{1+Z_C\left(\frac{v_p\Delta t}{\Delta z}\right)\left(\frac{1}{2R}+\frac{C}{\Delta t}\right)}}$$

and

$$\boxed{A_2=\frac{1}{1+Z_C\left(\frac{v_p\Delta t}{\Delta z}\right)\left(\frac{1}{2R}+\frac{C}{\Delta t}\right)}}.$$

Note that the update equation for the current is unchanged from that for a 1D lossless transmission line. However, there is now an intermediate auxiliary equation to update the current through the parallel inductor *L*. The voltage update equation (when compared to that for a 1D lossless transmission line) is significantly modified- an additional term to account for the current through *L*, coefficients that account for the parallel resistor *R* and capacitor *C* load in parallel, and is missing a term for the current node beyond the terminating load. Also, the terminating parallel RLC load is located at $z=(k+1)\Delta z=k_{\mathrm{LD}}\Delta z$ in the FDTD grid.

Verification of FDTD Update Equations for voltage sources and terminating RLC Loads

To demonstrate the validity of the derived FDTD update equations voltage sources and terminating RLC loads, a series of simple transmission line circuits incorporating all of the types of voltage sources and terminating RLC loads were modeled. The source voltage and voltage at the input of each transmission line circuit were examined (see Figures 6 - 11). The time axes were normalized (i.e., t/T) by the one-way transit time of the transmission line $T = \mathcal{L}/c$.

The FDTD results are compared with numerically derived results. To obtain the numerically derived results, frequency-domain lossless transmission line theory was used to obtain the input impedance looking into the transmission line. Then, a simple equivalent circuit model (i.e., voltage division), the spectrum of the applied voltage, and an inverse Fourier transform were used to find the input voltage. For these examples, a time-delayed, unit-amplitude, Gaussian-pulse voltage source was used

$$v_S(t) = e^{-0.5(t-\tau_d)^2/\tau_p^2},$$

where τ_p is the characteristic time and τ_d is a time delay.

The RLC element values were arbitrarily selected so that the contribution from each element type was evident. In the FDTD models, the transmission line ($Z_C = 50\ \Omega$, $v_p = 2.998 \times 10^8$ m/s, $\mathcal{L}$ = 0.04 m), Δz = 0.5 mm, τ_p = 16.732 ps, and S = 0.5. The time delay τ_d was selected to place the peak of $v_S(t)$ at $t/T = 1$.

Figures 6 – 9 show examples of series RLC voltage sources and series RLC terminating loads. As shown, there is excellent agreement between the analytic and FDTD results. Figures 10 – 11 show examples of parallel RLC voltage sources and parallel RLC terminating loads. As shown, there is good agreement between the analytic and FDTD results.

References

[1] J.G. Maloney, K.L. Shlager, and G.S. Smith, ``A Simple FDTD Model for Transient Excitation of Antennas by Transmission Lines," *IEEE Trans. Antennas Propagation*, vol. 42, no. 2, pp. 289-292, Feb. 1994.

[2] T. P. Montoya and G. S. Smith, "Modeling Transmission Line Circuit Elements in the FDTD Method," *Microwave and Optical Technology Letters*, vol. 21, no. 7, pp.105-114, April 20, 1999.

[3] T. P. Montoya and W. R. Scott, Jr., "Modeling Parallel and Series RLC Loads in a 1-D FDTD Transmission Line," *USNC/URSI National Radio Science Meeting*, Salt Lake City, UT, p. 30, July 16-21, 2000.

[4] T. P. Montoya, "Improved 1-D FDTD Modeling of Parallel and Series RLC Loads in a Lossless Transmission Line," 2006 *IEEE APS International Symp.*, Albuquerque, NM, pp. 1583-1586, July 9-14, 2006.

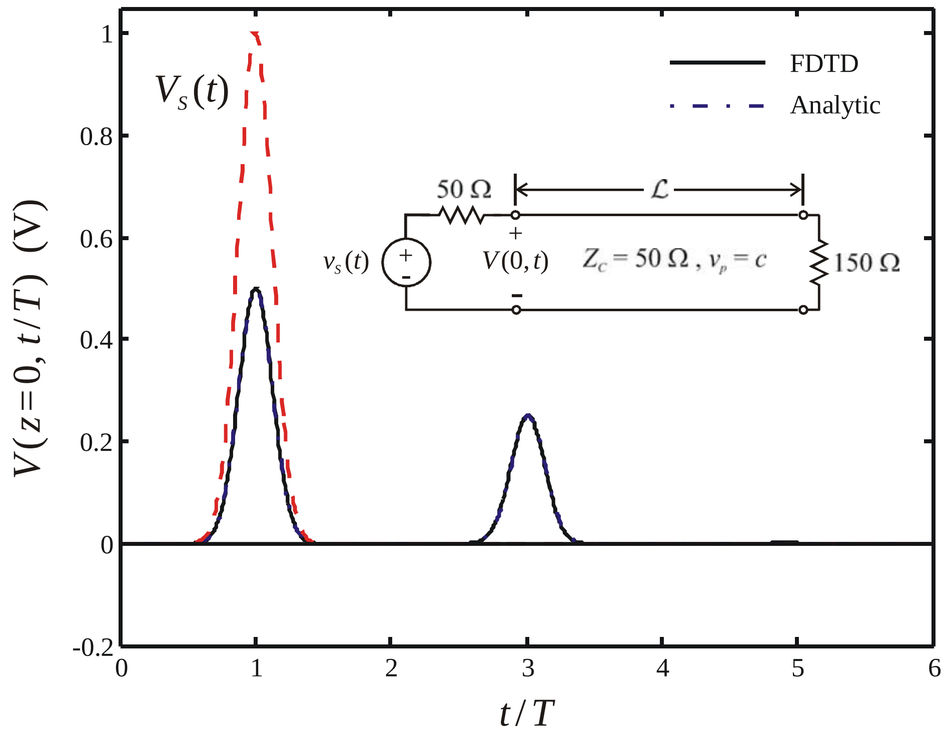

Figure 6 Source voltage, $v_S(t)$, and input voltage, $V(0, t)$, for a transmission line circuit consisting of a matched voltage source, a lossless transmission line section, and a mismatched resistive terminating load.

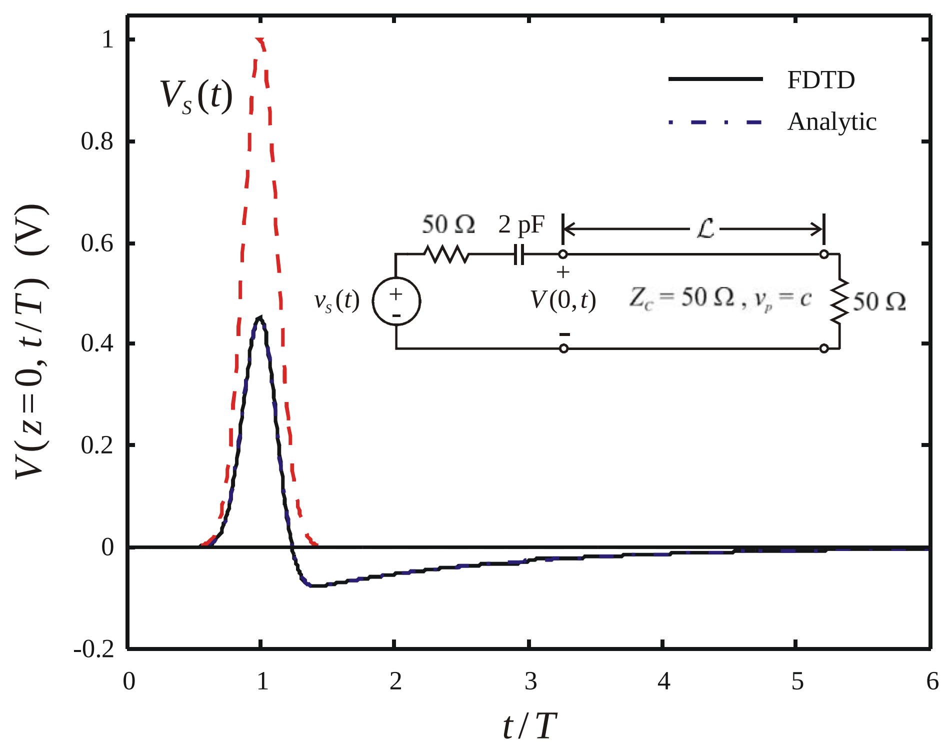

Figure 7 Source voltage, $v_S(t)$, and input voltage, $V(0, t)$, for a transmission line circuit consisting of a series RC voltage source, a lossless transmission line section, and a matched resistive terminating load.

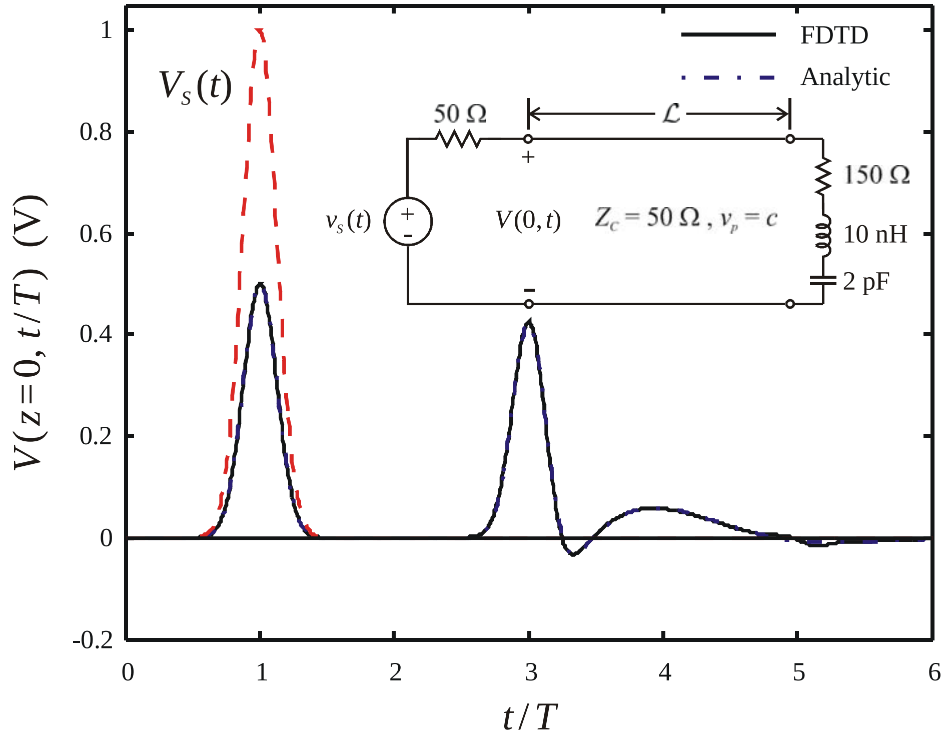

Figure 8 Source voltage, $v_S(t)$, and input voltage, $V(0, t)$, for a transmission line circuit consisting of a matched voltage source, a lossless transmission line section, and a series RLC terminating load.

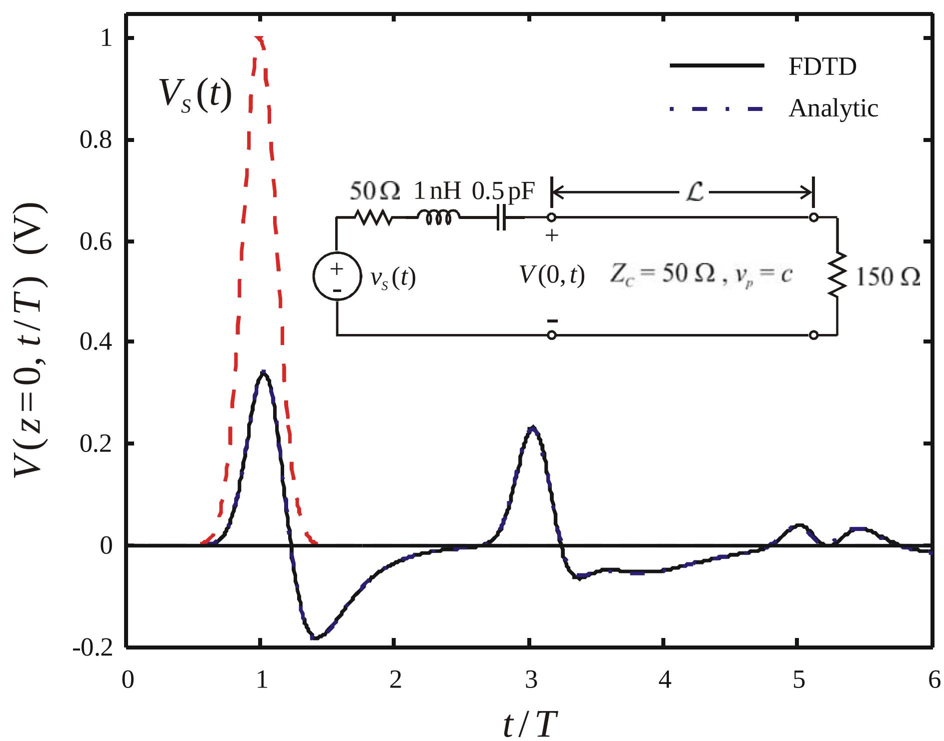

Figure 9 Source voltage, $v_S(t)$, and input voltage, $V(0, t)$, for a transmission line circuit consisting of a series RLC voltage source, a lossless transmission line section, and a mismatched resistive terminating load.

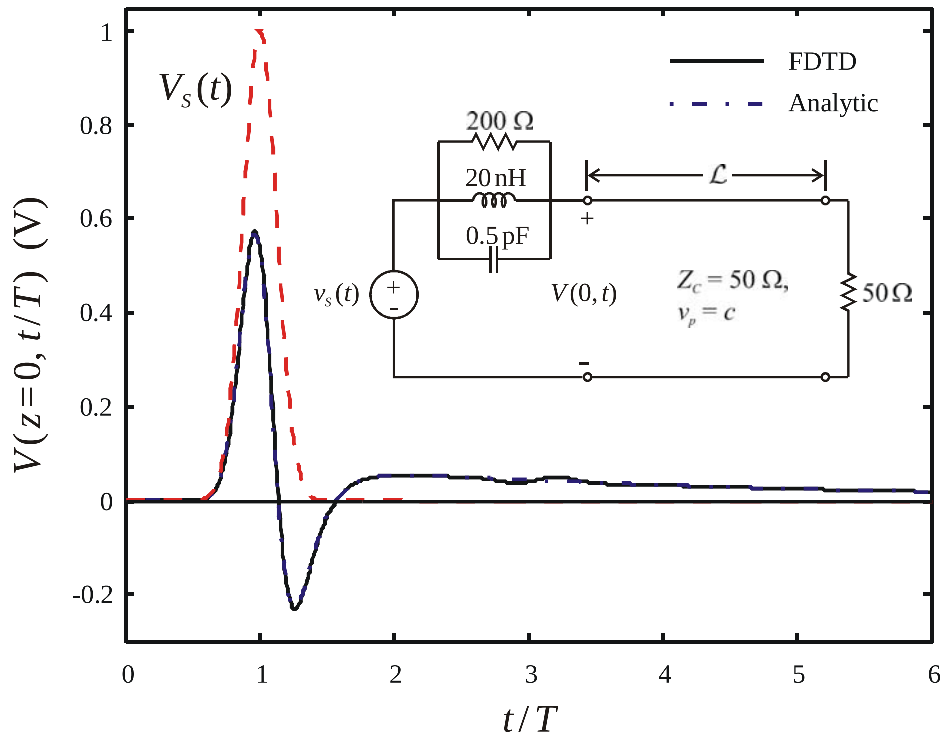

Figure 10 Source voltage, $v_S(t)$, and input voltage, $V(0, t)$, for a transmission line circuit consisting of a parallel RLC voltage source, a lossless transmission line section, and a matched resistive terminating load.

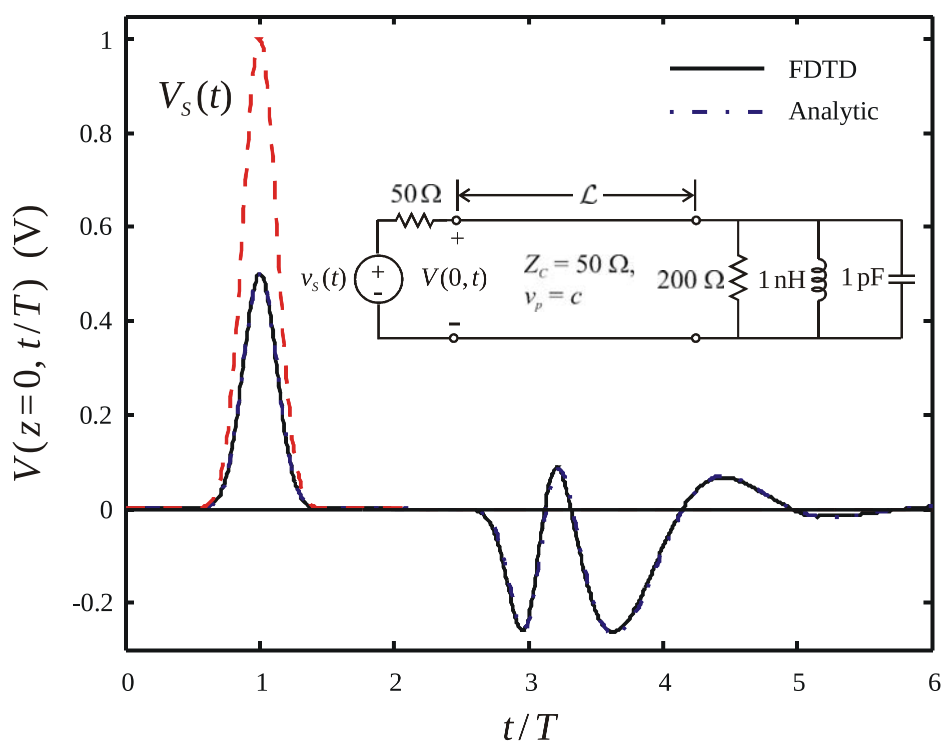

Figure 11 Source voltage, $v_S(t)$, and input voltage, $V(0, t)$, for a transmission line circuit consisting of a matched voltage source, a lossless transmission line section, and a parallel RLC terminating load.