

## EE 481/581 Microwave Engineering (Fall 2024)

### Homework 12

Tuesday, December 3, 2024

- 1) 8.13 a) Find and make fully-labeled sketch of low-pass filter prototype circuit (use form shown in Fig. 8.25b with Thevenin equivalent source). b) Use Richards' Transformation to implement low-pass filter prototype using stubs and draw fully-labeled sketch of resulting circuit. c) Add unit element to the lefthand side, sketch resulting circuit, apply Kuroda identity, & sketch resulting circuit. d) Add a unit element to the righthand side by load, sketch resulting circuit, apply Kuroda identity, & sketch resulting circuit. e) Add a unit element to the righthand side by load (again), sketch resulting circuit, apply Kuroda identity to each of the two resulting short-circuit stub & unit element combinations, and sketch resulting circuit. [Normalized design should now only have shunt open-circuit stubs.] f) Scale all impedances to a 50  $\Omega$  system and draw a fully-labeled sketch of final design. For all steps, the lengths  $\ell$  may be left in terms of  $\lambda$  at  $f_c$ . CAD part is not required.
- 2) 8.16a First, find and draw fully-labeled sketch of low-pass filter prototype circuit (use form shown in Fig. 8.25a). Also, specify the impedance associated with each section. CAD part is not required.
- 3) Use MWI program to design a microstrip implementation of the stepped-impedance low-pass filter designed in 8.16a on Rogers RO4003C with 1 oz. copper and 0.06" board thickness. [Hint: Use 'Dk values for characteristic impedance' option.] a) Find width  $w_{15}$ , phase velocity  $w_{15}$ , wavelength  $\lambda_{15}$ , and length  $\ell_{15}$  of 15  $\Omega$  sections. b) Find width  $w_{120}$ , phase velocity  $w_{120}$ , wavelength  $\lambda_{120}$ , and length  $\ell_{120}$  of 120  $\Omega$  sections. c) Find width  $w_{50}$ , phase velocity  $w_{50}$ , and wavelength  $\lambda_{50}$  for 50  $\Omega$  microstrip. d) Draw a fully-labeled top view sketch of design with 50  $\Omega$  microstrip traces (indefinite length) at input and output. For legibility, the sketch may be scaled.

➤ Include any design figures/tables used.

**Due Friday, December 6, 2024 by 4 pm at my office or EECS mail box.**