Section 10.1.1 Energy-Band Diagrams

[and MOS capacitors]

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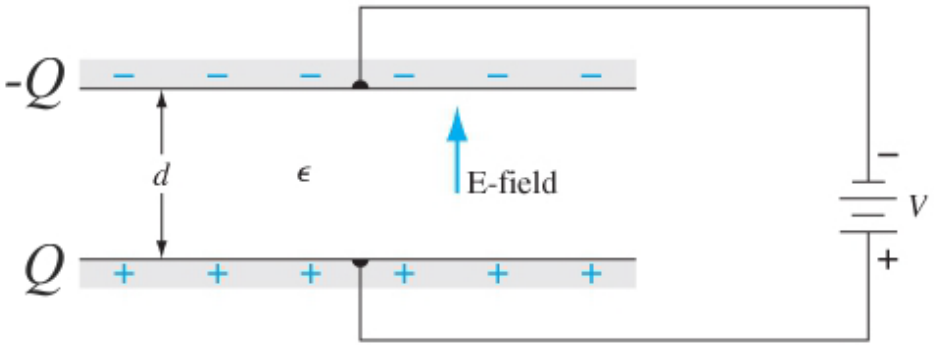


Figure 10.2 | (a) A parallel-plate capacitor showing the electric field and conductor charges.

- As a review, a **parallel-plate capacitor** is shown above. The voltage source moves negative charges to the top plate and positive charges to the bottom plate.
- The linear relationship between positive stored charge Q and the applied voltage V is given by $Q = C\,V$ where C is the capacitance (F).
- For a parallel-plate capacitor, the capacitance is $C = \varepsilon A/d$ (F) and the electric field is $E = V/d$ (V/m or V/cm).
- The capacitance-per-unit-area is $C' = \varepsilon/d$ (F/m^2 or F/cm^2) which leads to the charge-per-unit-area $Q' = C'\,V$ (C/m^2 or C/cm^2).

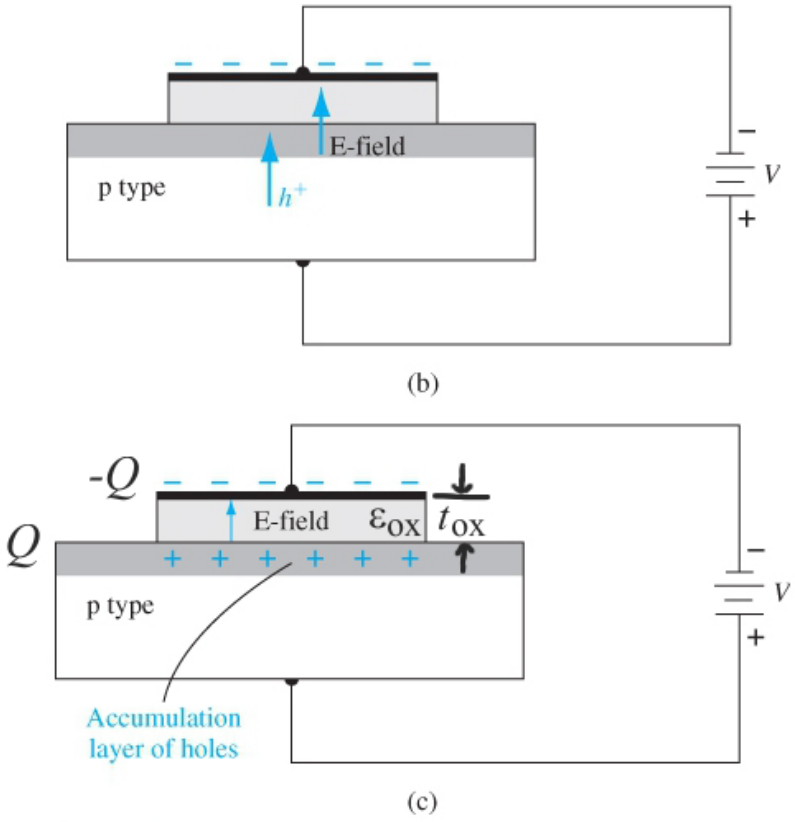


Figure 10.2 | (b) A corresponding MOS capacitor with a negative gate bias showing the electric field and charge flow. (c) The MOS capacitor with an accumulation layer of holes.

- Next, a **MOS capacitor** is shown above. As shown in (b), the voltage source moves negative charges to the top plate and holes (positive charges) from the p type semiconductor substrate toward the bottom boundary of the oxide layer.
- At steady-state as shown in Fig 10.2(c), there is a linear relationship between positive stored charge Q (in what is called the **accumulation layer**) and applied voltage V given by $Q = C\,V$.
- Here, $C = \varepsilon_{ox} A / t_{ox}$ (F) and the electric field <u>in the oxide</u> is $E = V / t_{ox}$ (V/m or V/cm). [As before, $E \sim 0$ in the p type substrate.]
- On a per-unit-area basis, we have $C' = \varepsilon_{ox} / t_{ox}$ (F/m^2 or F/cm^2) and $Q' = C'\,V$ (C/m^2 or C/cm^2).

What happens if the voltage is reversed on the MOS capacitor as shown in Fig 10.3?

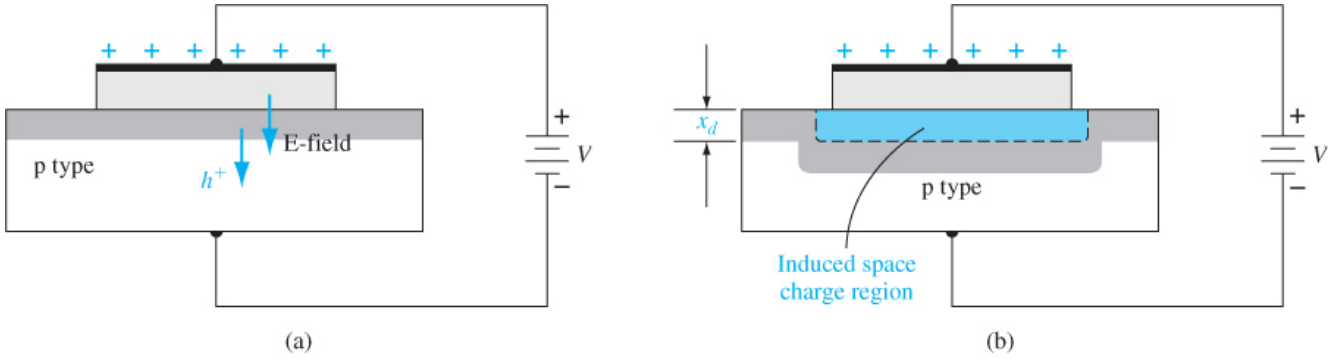


Figure 10.3 | The MOS capacitor with a moderate positive gate bias, showing (a) the electric field and charge flow and (b) the induced space charge region.

- As shown in (a), the voltage source moves positive charges to the top plate (will be called the **gate**). The holes (positive charges) in the p type substrate will move away from the bottom boundary of the oxide layer.
- At steady-state as shown in Fig 10.3(b), an **induced space charge region** or **depletion layer** (w/ N_a^- ions) of width/thickness x_d is formed (not like a parallel plate capacitor).

What happens to the energy bands in the p type semiconductor substrate?

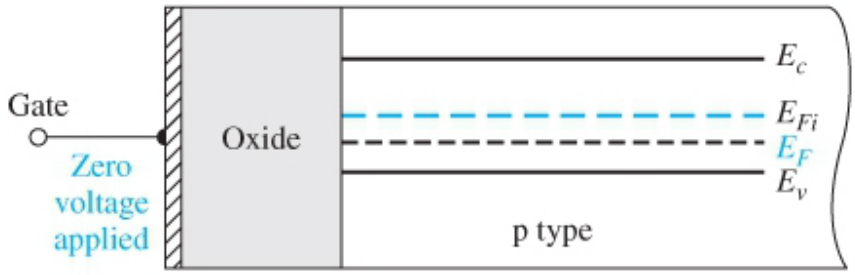
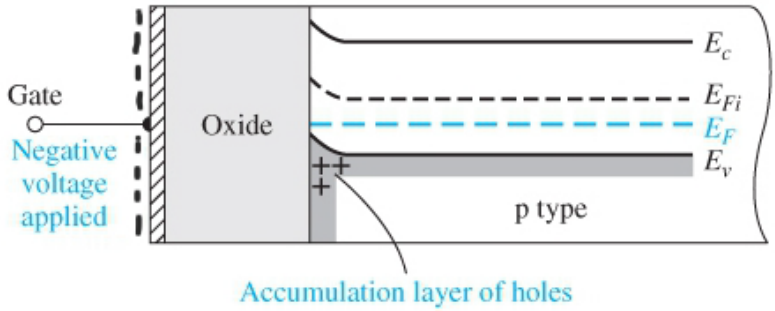


Figure 10.4 | The energy-band diagram of a MOS capacitor with a p-type substrate for (a) a zero applied gate bias showing the *ideal* case,

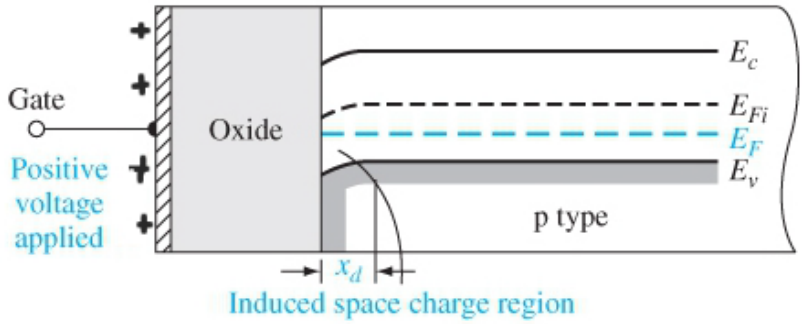
- With no applied voltage at the gate (metal plate), the energy bands are flat with respect to position in the p type semiconductor substrate.
- Note that $E_F < E_{Fi}$, i.e., E_F is closer to E_v than to E_c, as one would expect for a p type semiconductor.



(b)

Figure 10.4 | The energy-band diagram of a MOS capacitor with a p-type substrate for (b) a negative gate bias

- With a negative voltage applied at the gate (Fig. 10.4b), there is an accumulation layer of holes near the oxide to p type semiconductor substrate boundary. This region is more strongly 'p type' than the rest of the substrate.
- Therefore, E_F (remains flat) must be closer to E_v than before. This results in E_c, E_v, and E_{Fi} bending up near the boundary (while maintaining their spacing).



(c)

Figure 10.4 | The energy-band diagram of a MOS capacitor with a p-type substrate for (c) a moderate positive gate bias.

- With a positive voltage applied at the gate (Fig. 10.4c), there is a depletion layer (w/ N_a^- ions) near the oxide to p type substrate boundary. This region, with fewer holes, is less 'p type' than the rest of the substrate.
- Therefore, E_F (remains flat) must be further from E_v than before. This results in E_c, E_v, and E_{Fi} bending down near the boundary (while maintaining their spacing).
- The width/depth/thickness of the depletion layer x_d is roughly the depth that the electric field E now penetrates into the p type substrate.

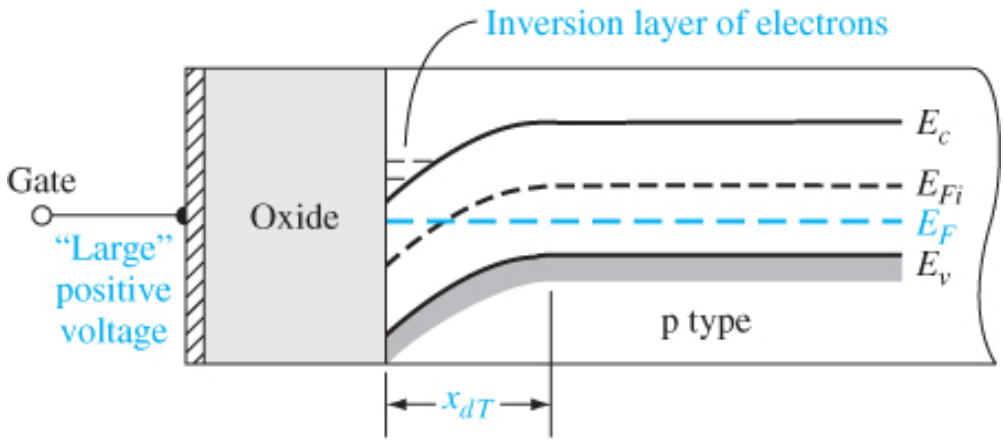


Figure 10.5 | The energy-band diagram of the MOS capacitor with a p-type substrate for a "large" positive gate bias.

- When a 'large' positive voltage applied at the gate (Fig. 10.5), there is a maximally thick depletion layer adjacent to the oxide/substrate boundary.
- Again, E_F (remains flat) is even further from E_v than before. This results in E_c, E_v, and E_{Fi} bending down near the boundary (while maintaining their spacing).
- In addition, $E_F > E_{Fi}$ and E_F gets closer to E_c than E_v near the boundary. E_F remains closer to E_v in the bulk p type substrate away from boundary.
- The width/depth/thickness of the depletion layer x_{dT} is roughly the depth that the electric field E penetrates into the p type substrate.
- Now, enough electrons make it through the depletion layer to accumulate near the boundary, forming what is called an **inversion layer**, and, by definition, the semiconductor substrate is **n type** in the region where $\boldsymbol{E_F > E_{Fi}}$!

Similar phenomenon occurs with an **n type substrate** (voltages & charges reversed).

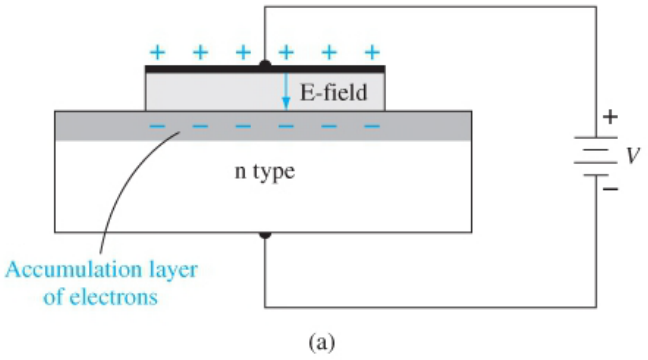


Figure 10.6 | The MOS capacitor with an n-type substrate for (a) a positive gate bias

- A **MOS capacitor** with an n type semiconductor substrate is shown above in Fig. 10.6a. The voltage source (positive at gate) moves positive charges to the top plate and electrons (negative charges) from the n type semiconductor substrate toward the bottom boundary of the oxide layer (**accumulation layer**).
- At steady-state, there is a linear relationship between positive stored charge Q and applied voltage V given by $Q = C\,V$.
- Here, $C = \varepsilon_{ox} A / t_{ox}$ (F) and the electric field in the oxide is $E = V / t_{ox}$ (V/m or V/cm). [As before, $E \sim 0$ in the n type substrate.]
- On a per-unit-area basis, we have $C' = \varepsilon_{ox} / t_{ox}$ (F/m^2 or F/cm^2) and $Q' = C'\,V$ (C/m^2 or C/cm^2).

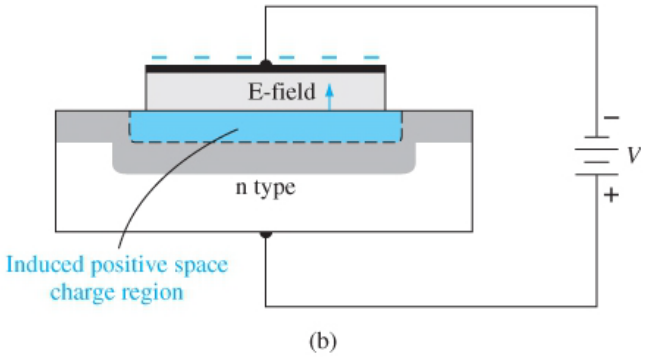
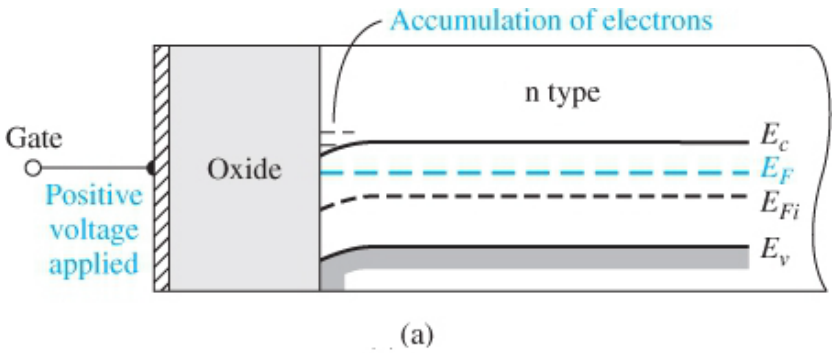


Figure 10.6 | The MOS capacitor with an n-type substrate for (b) a moderate negative gate bias.

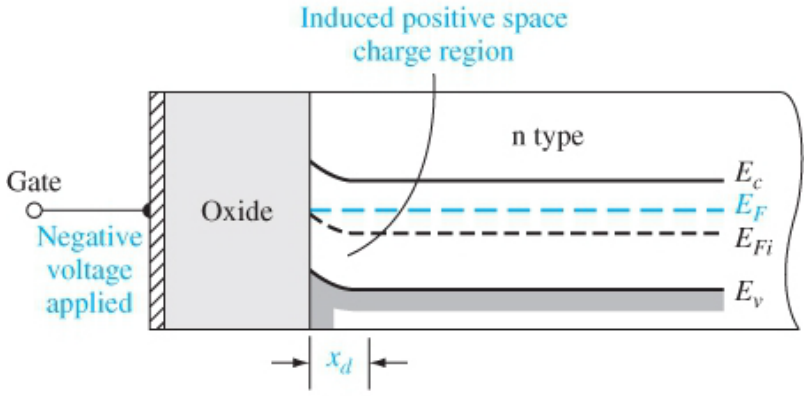
- However, when a negative voltage is applied to the gate as shown in Fig. 10.6b, the voltage source moves negative charges to the top plate/**gate**. The electrons (negative charges) in the n type semiconductor substrate will move away from the bottom boundary of the oxide layer forming an **induced space charge region** or **depletion layer** w/ N_d^+ ions (not like a parallel plate capacitor).



(a)

Figure 10.7 | The energy-band diagram of the MOS capacitor with an n-type substrate for (a) a positive gate bias,

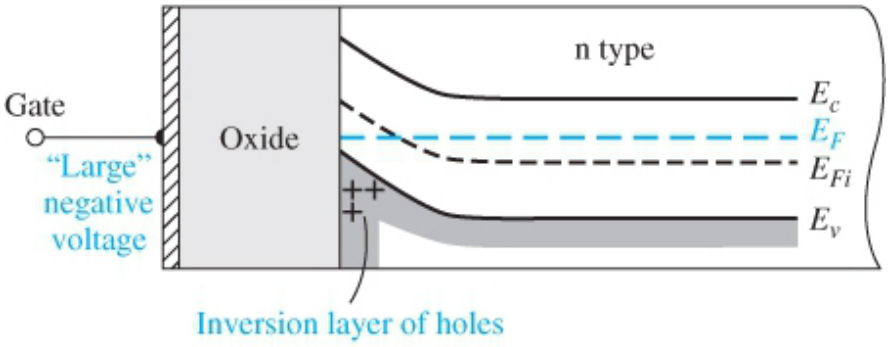
- With a **positive voltage** applied at the gate (Fig. 10.7a), there is an accumulation layer of electrons near the oxide to n type semiconductor substrate boundary. This region is more strongly 'n type' than the rest of the substrate.
- Therefore, E_F (remains flat) must be closer to E_c than before. This results in E_c, E_v, and E_{Fi} bending down near the boundary (while maintaining their spacing).



(b)

Figure 10.7 | The energy-band diagram of the MOS capacitor with an n-type substrate for (b) a moderate negative bias

- With a **negative voltage** applied at the gate (Fig. 10.7b), there is a depletion layer (w/ N_d^+ ions) near the oxide to n type substrate boundary. This region, with fewer electrons, is less 'n type' than the rest of the substrate.
- Therefore, E_F (remains flat) must be further from E_c than before. This results in E_c, E_v, and E_{Fi} bending up near the boundary (while maintaining their spacing).
- The width/depth/thickness of the depletion layer x_d is roughly the depth that the electric field E now penetrates into the n type substrate.



(c)

Figure 10.7 | The energy-band diagram of the MOS capacitor with an n-type substrate for (c) a "large" negative gate bias.

- When a 'large' negative voltage applied at the gate (Fig. 10.7c), there is a maximally thick depletion layer near the oxide to n type substrate boundary.
- Again, E_F (remains flat) is even further from E_c than before. This results in E_c, E_v, and E_{Fi} bending up near the boundary (while maintaining their spacing).
- In addition, $E_F < E_{Fi}$ and E_F gets closer to E_v than E_c near the boundary. E_F remains closer to E_c in the bulk n type substrate away from boundary.
- The width/depth/thickness of the depletion layer x_{dT} is roughly the depth that the electric field E penetrates into the n type substrate.
- Enough holes now make it through the depletion layer to accumulate near the boundary, forming what is called an **inversion layer**, and, by definition, the semiconductor substrate is **p type** in the region where $\boldsymbol{E_F < E_{Fi}}$!