From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.

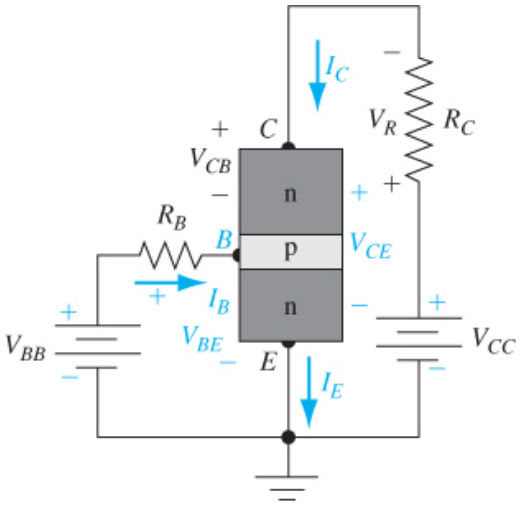

Figure 12.8 | An npn bipolar transistor in a common-emitter circuit configuration.

- BY KVL around the RH loop $V_{CC} = I_C R_C + V_{CB} + V_{BE} = V_R + V_{CE}$
- For $V_{BE} > 0$ (forward biased) with V_{CC} large enough and V_R small enough $V_{CB} > 0$ $\Rightarrow$ BC pn junction is reverse biased (active mode).
- As V_{BE} increases, $I_C = I_S e^{v_{BE}/V_t}$ increases. In turn, $V_R = I_C R_C$ increases enough that $V_{CB} \leq 0 \Rightarrow BC$ pn junction is forward biased (**saturation** mode). I_C does NOT depend on V_{BE} at this point and is essentially limited only by R_C, $I_C \rightarrow V_{CC}/R_C$.

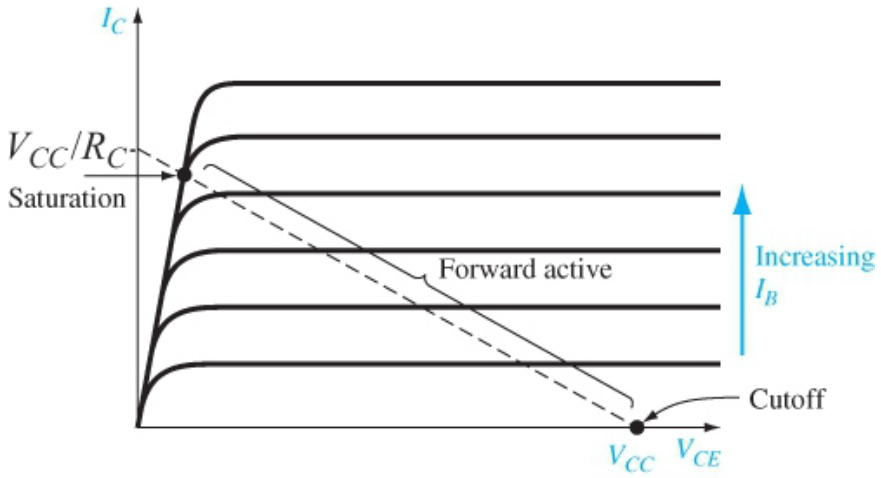

Figure 12.9 | Bipolar transistor common-emitter current–voltage characteristics with load line superimposed.

- BY KVL, $V_{CE} = V_{CC} - I_C R_C$. This is called the load line equation (dashed line in Figure 12.9).