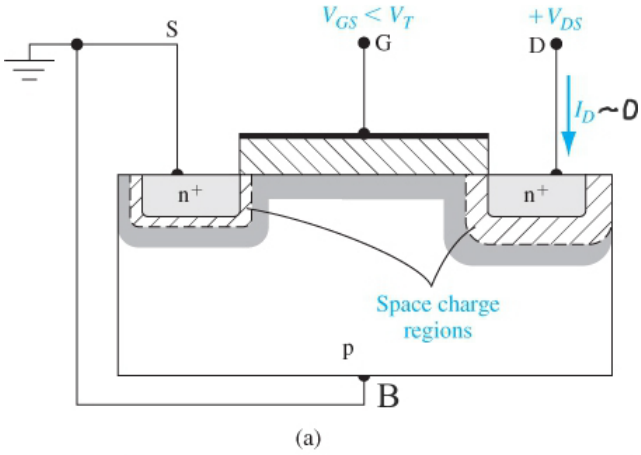
From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.

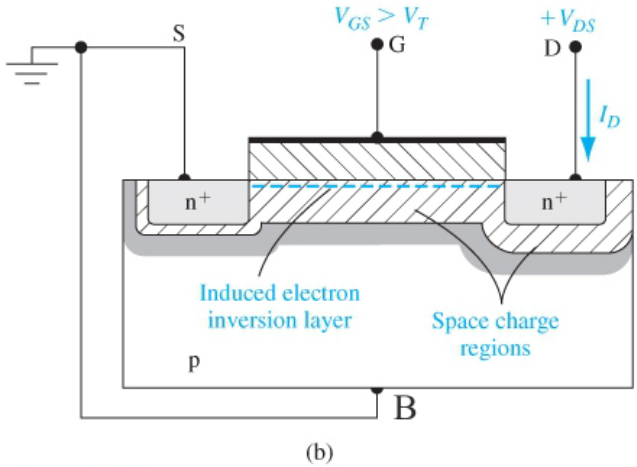
n-channel enhancement mode MOSFET



(a)

Figure 10.37 | The n-channel enhancement mode MOSFET
(a) with an applied gate voltage $V_{GS} < V_T$

- Note that the source (S) and body (B) are tied together and grounded.
- Note that the gate (G) voltage V_G has been renamed V_{GS} while the drain (D) voltage has been renamed V_{DS}, this indicates they are referenced to ground (node voltages).
- With $V_{GS} < V_T$, there is no inversion layer (AKA n channel). In fact, there is a depletion layer (space charge region) between the n^+ drain and source and the p-type substrate. Therefore, $I_D \sim 0$ (ignore leakage) even with $V_{DS} > 0$.



(b)

Figure 10.37 | The n-channel enhancement mode MOSFET
(b) with an applied gate voltage $V_{GS} > V_T$.

- With $V_{GS} > V_T$, there is an inversion layer (AKA n channel). Therefore, $I_D > 0$ with $V_{DS} > 0$. [Reality: electrons to flow from the source to the drain.]

Reality- can't just keep increasing V_{DS} with a corresponding linear increase in I_D.

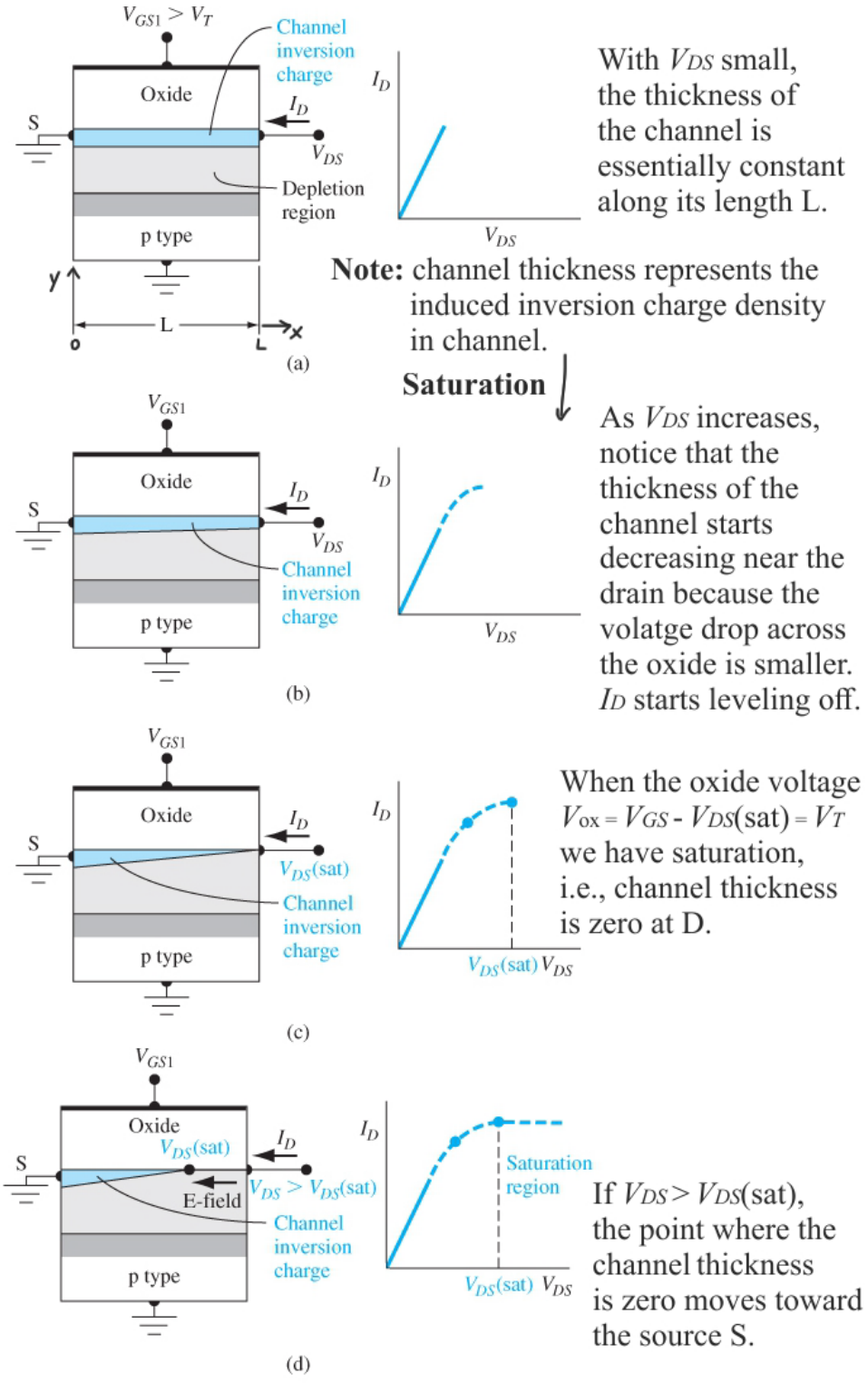


Figure 10.39 | Cross section and I_D versus V_{DS} curve when $V_{GS} < V_T$ for (a) a small V_{DS} value, (b) a larger V_{DS} value, (c) a value of $V_{DS} = V_{DS}$(sat), and (d) a value of $V_{DS} > V_{DS}$(sat).

- Saturation voltage $\underline{\boldsymbol{V_{DS}\,(sat) = V_{GS} - V_T}}$. Saturation is a reason to set V_{GS} greater than the minimum required to achieve threshold, i.e., set $V_{GS} > V_T$.