From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.
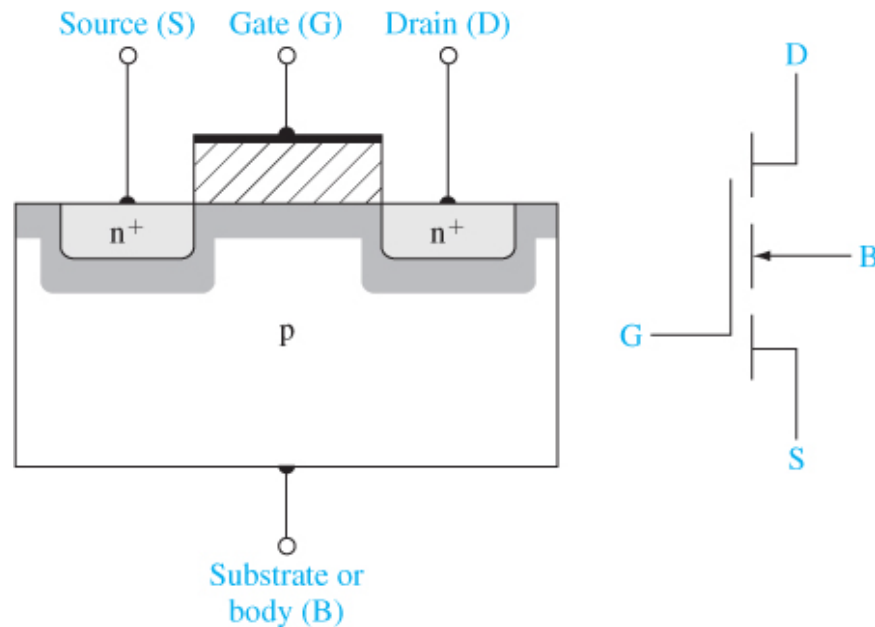
n-channel enhancement mode MOSFET

Figure 10.34 | Cross section and circuit symbol for an n-channel enhancement mode MOSFET.

➤ There is NOT an inversion layer when the gate voltage is zero ($V_G = 0$).

➤ A positive gate voltage ($V_G > 0$, e.g., $V_G = V_T$) induces an n-type inversion layer in the p-type substrate below the **Gate** (G) which creates a path connecting the n-type **Source** (S) and n-type **Drain** (D) for electrons to flow from the source to the drain, i.e., conventional current flows from D to S (opposite).

➤ Circuit symbol is shown to the right. Note that there are separate lines touching D, S, and the **Body** (B). This is to indicate that there is NOT an n channel when $V_G = 0$.
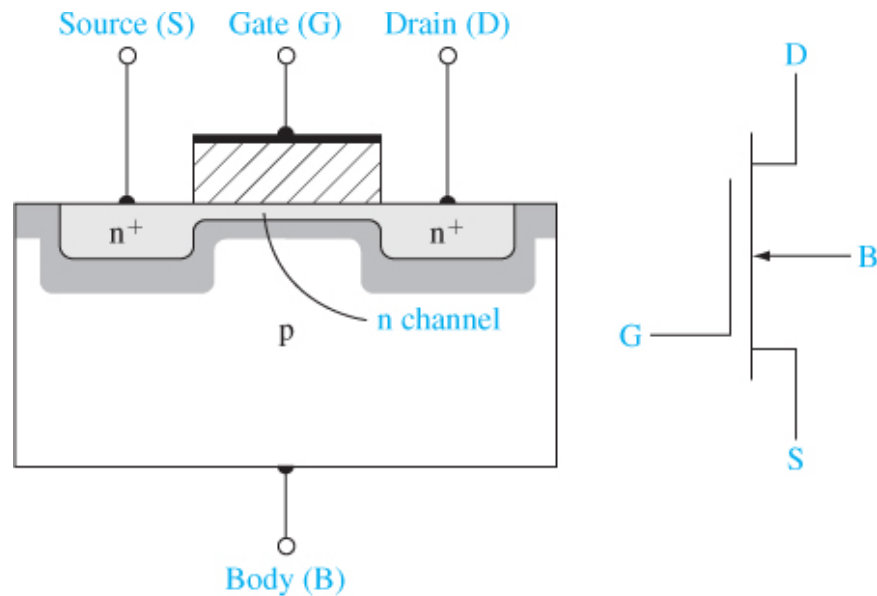
n-channel depletion mode MOSFET

Figure 10.35 | Cross section and circuit symbol for an n-channel depletion mode MOSFET.

➢ There IS an inversion layer when the gate voltage is zero ($V_G = 0$).

➢ The n channel can be an n-type inversion layer **or** an intentionally doped n region.

➢ There is a path connecting the source and drain for <u>electrons</u> to flow from the source to the drain, i.e., conventional current flows from the drain to the source.

➢ Circuit symbol is shown to the right. Note that there is a <u>single</u> line touching D, S, and B to indicate the existence of the n channel with $V_G = 0$.
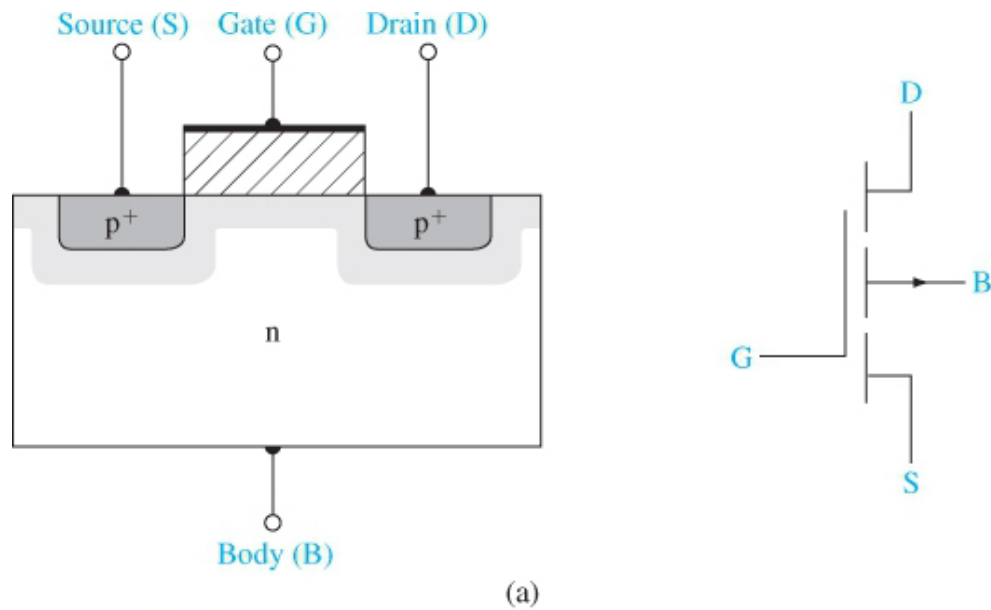
p-channel enhancement mode MOSFET

Figure 10.36 | Cross section and circuit symbol for (a) a p-channel enhancement mode MOSFET

➢ There is NOT an inversion layer when the gate voltage is zero ($V_G = 0$).

➢ A negative gate voltage ($V_G < 0$, e.g., $V_G = V_T$) induces an p-type inversion layer in the n-type substrate below the **Gate** (G) which creates a path connecting the p-type **Source** (S) and p-type **Drain** (D) for <u>holes</u> to flow from the source to the drain, i.e., conventional current flows from S to D (same).

➢ Circuit symbol is shown to the right. Note that there are <u>separate</u> lines touching D, S, and the **Body** (B). This is to indicate that there is NOT a p channel when $V_G = 0$.
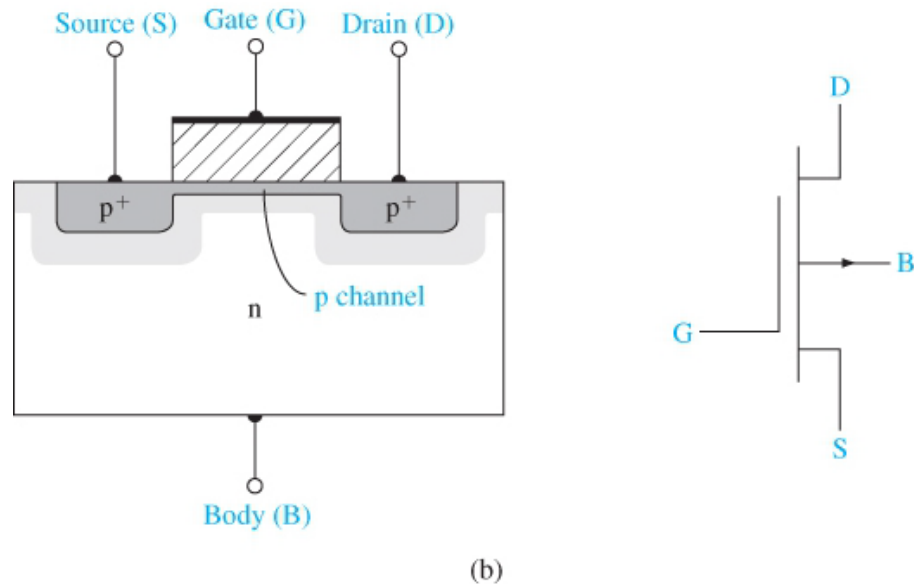
n-channel depletion mode MOSFET

(b)

Figure 10.36 | Cross section and circuit symbol for (b) a p-channel
depletion mode MOSFET.

➢ There IS an inversion layer when the gate voltage is zero ($V_G = 0$).

➢ The p channel can be an p-type inversion layer **or** an intentionally doped p region.

➢ There is a path connecting the source and drain for <u>holes</u> to flow from the source to the drain, i.e., conventional current flows from S to D (same).

➢ Circuit symbol is shown to the right. Note that there is a <u>single</u> line touching D, S, and B to indicate the existence of the p channel with $V_G = 0$.