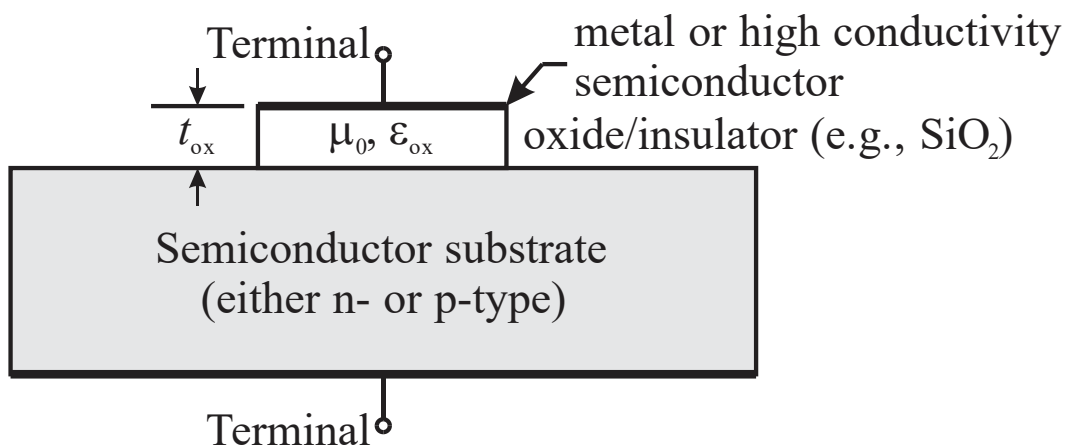


Chapter 10 Fundamentals of the MOSFET

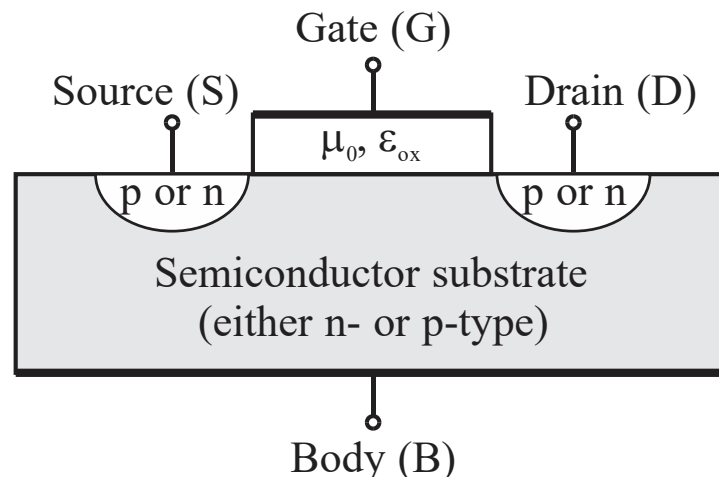
- **MOSFET** ≡ **Metal-Oxide-Semiconductor Field-Effect-Transistor**
- Two complementary types of MOSFETs: n-channel and p-channel
- Using both types of MOSFETs leads to complementary MOS (CMOS) circuits/device

10.1 The Two-Terminal MOS Structure

- Start with the MOS capacitor



- **Preview-** This MOS capacitor will later be turned into a MOSFET by adding two regions (called **Source** and **Drain**) to the substrate on either side of the oxide layer with doping opposite to the main body of the substrate.



10.1.1 Energy-Band Diagrams

[and MOS capacitors]

From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.

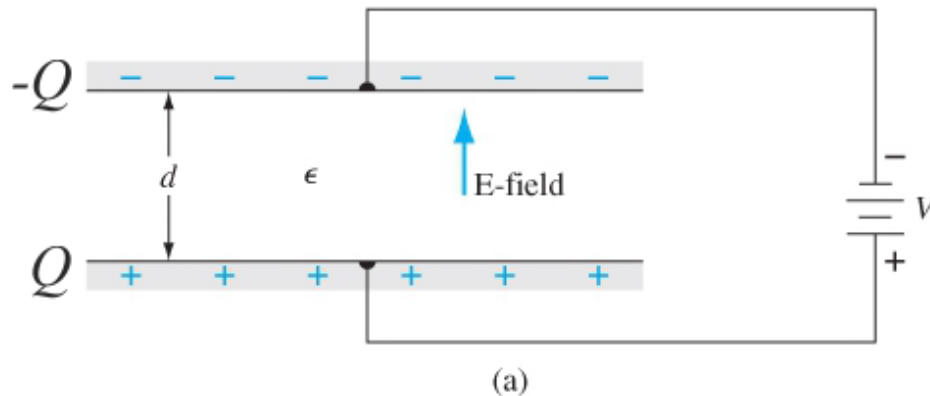


Figure 10.2 | (a) A parallel-plate capacitor showing the electric field and conductor charges.

- As a review, a **parallel-plate capacitor** is shown above. The voltage source moves negative charges to the top plate and positive charges to the bottom plate.
- The linear relationship between positive stored charge Q and the applied voltage V is given by $Q = CV$ where C is the capacitance (F).
- For a parallel-plate capacitor, the capacitance is $C = \epsilon A/d$ (F) and the electric field is $E = V/d$ (V/m or V/cm).
- The capacitance-per-unit-area is $C' = \epsilon/d$ (F/m² or F/cm²) which leads to the charge-per-unit-area $Q' = C'V$ (C/m² or C/cm²).

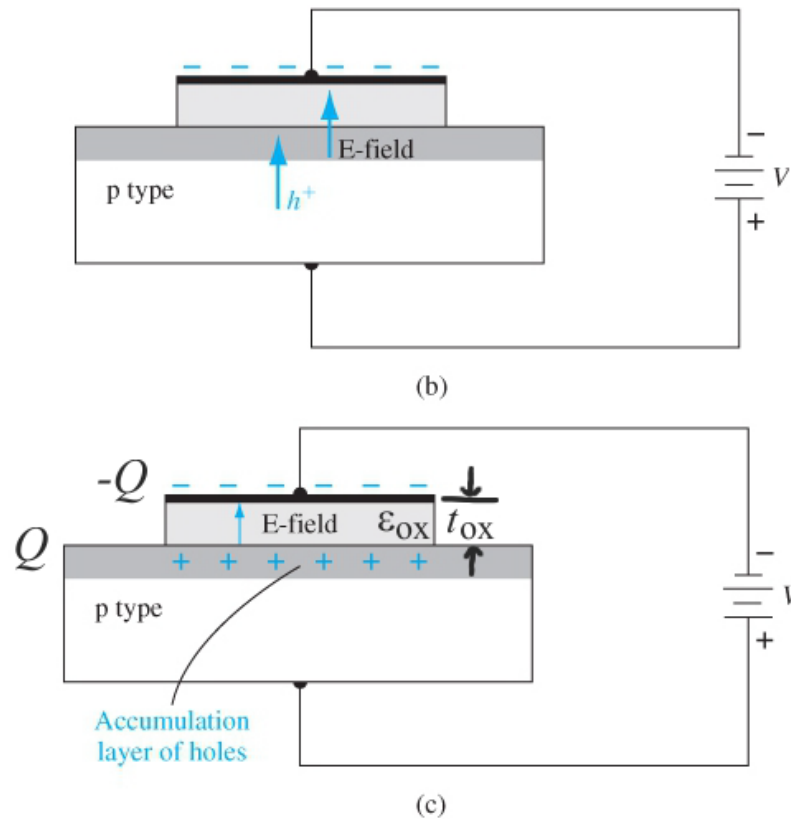


Figure 10.2 | (b) A corresponding MOS capacitor with a negative gate bias showing the electric field and charge flow. (c) The MOS capacitor with an accumulation layer of holes.

- Next, a **MOS capacitor** is shown above. As shown in (b), the voltage source moves negative charges to the top plate and holes (positive charges) from the p type semiconductor substrate toward the bottom boundary of the oxide layer.
- At steady-state as shown in Fig 10.2(c), there is a linear relationship between positive stored charge Q (in what is called the **accumulation layer**) and applied voltage V given by $Q = CV$.
- Here, $C = \epsilon_{ox} A / t_{ox}$ (F) and the electric field in the oxide is $E = V / t_{ox}$ (V/m or V/cm). [As before, $E \sim 0$ in the p type substrate.]
- On a per-unit-area basis, we have $C' = \epsilon_{ox} / t_{ox}$ (F/m² or F/cm²) and $Q' = C'V$ (C/m² or C/cm²).

What happens if the voltage is reversed on the MOS capacitor as shown in Figure 10.3?

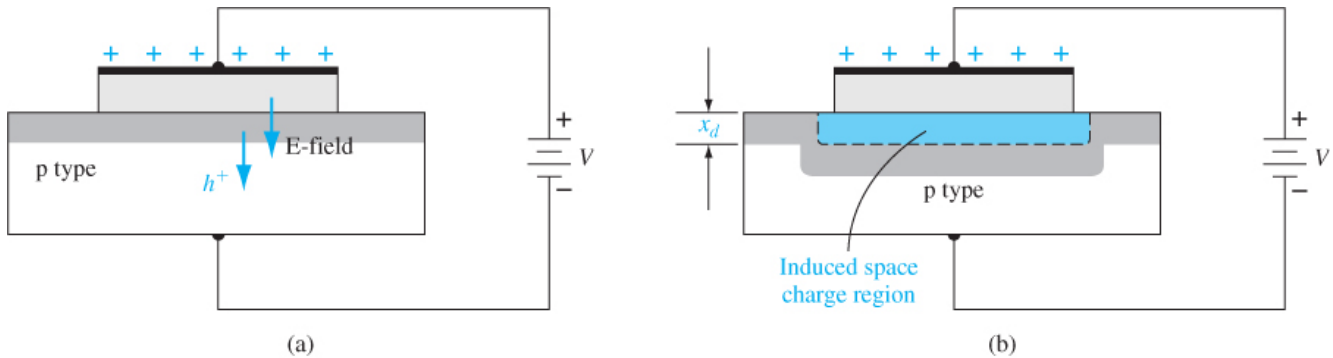


Figure 10.3 | The MOS capacitor with a moderate positive gate bias, showing (a) the electric field and charge flow and (b) the induced space charge region.

- As shown in (a), the voltage source moves positive charges to the top plate (will be called the **gate**). The holes (positive charges) in the p type substrate will move away from the bottom boundary of the oxide layer.
- At steady-state as shown in Fig 10.3(b), an **induced space charge region** or **depletion layer** (w/ N_a^- ions) of width/thickness x_d is formed (not like a parallel plate capacitor).

What happens to the energy bands in the p type semiconductor substrate?

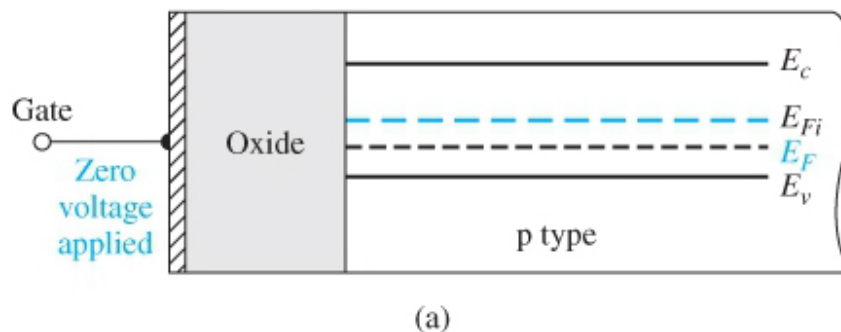


Figure 10.4 | The energy-band diagram of a MOS capacitor with a p-type substrate for (a) a zero applied gate bias showing the *ideal* case,

- With no applied voltage at the gate (metal plate), the energy bands are flat with respect to position in the p type semiconductor substrate.
- Note that $E_F < E_{Fi}$, i.e., E_F is closer to E_v than to E_c , as one would expect for a p type semiconductor.

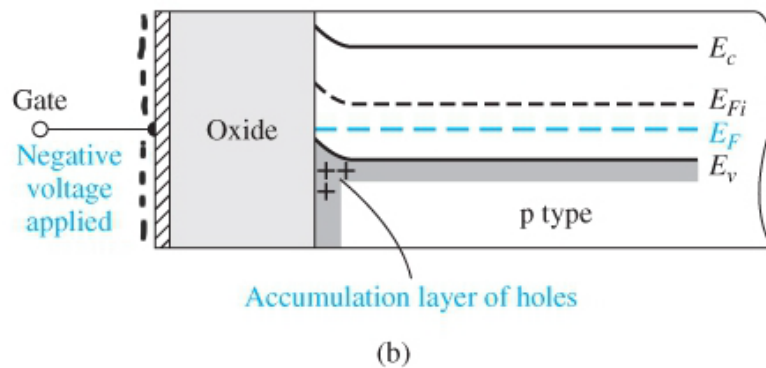


Figure 10.4 | The energy-band diagram of a MOS capacitor with a p-type substrate for (b) a negative gate bias

- With a negative voltage applied at the gate (Fig. 10.4b), there is an accumulation layer of holes near the oxide to p type semiconductor substrate boundary. This region is more strongly ‘p type’ than the rest of the substrate.
- Therefore, E_F (remains flat) must be closer to E_v than before. This results in E_c , E_v , and E_{Fi} bending up near the boundary (while maintaining their spacing).

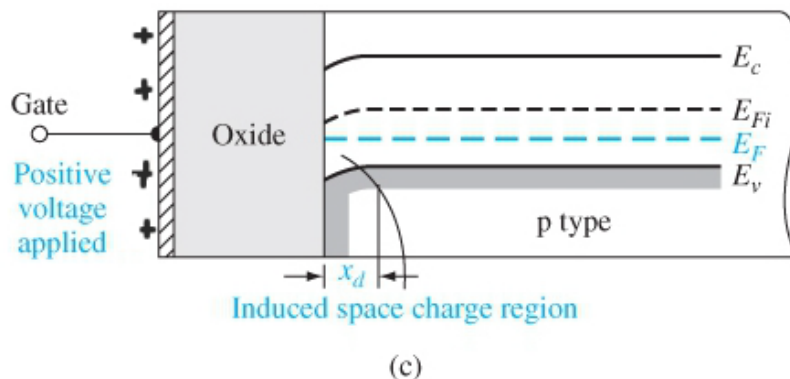


Figure 10.4 | The energy-band diagram of a MOS capacitor with a p-type substrate for (c) a moderate positive gate bias.

- With a positive voltage applied at the gate (Fig. 10.4c), there is a depletion layer (w/ Na^- ions) near the oxide to p type substrate boundary. This region, with fewer holes, is less ‘p type’ than the rest of the substrate.
- Therefore, E_F (remains flat) must be further from E_v than before. This results in E_c , E_v , and E_{Fi} bending down near the boundary (while maintaining their spacing).
- The width/depth/thickness of the depletion layer x_d is roughly the depth that the electric field E now penetrates into the p type substrate.

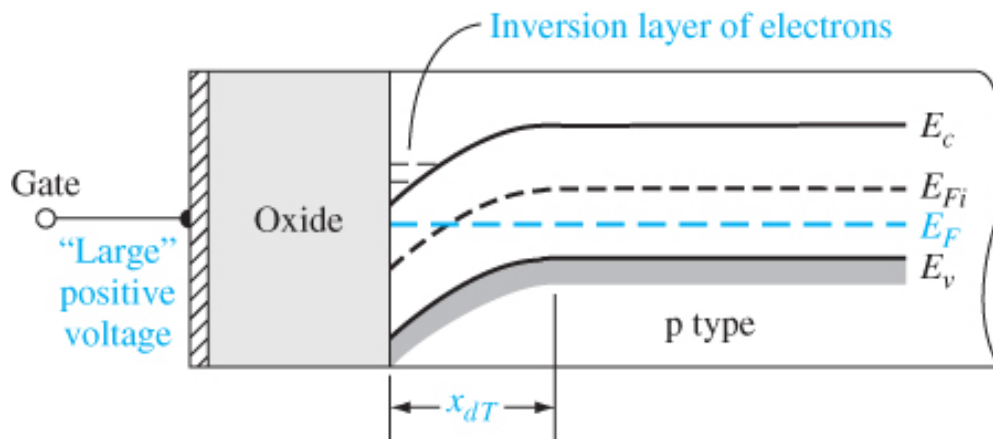


Figure 10.5 | The energy-band diagram of the MOS capacitor with a p-type substrate for a “large” positive gate bias.

- When a ‘large’ positive voltage applied at the gate (Fig. 10.5), there is a maximally thick (x_{dT}) depletion layer adjacent to the oxide/substrate boundary.
- Again, E_F (remains flat) is even further from E_v than before. This results in E_c , E_v , and E_{Fi} bending down near the boundary (while maintaining their spacing).
- In addition, $E_F > E_{Fi}$ and E_F gets closer to E_c than E_v near the boundary. E_F remains closer to E_v in the bulk p type substrate away from boundary.
- The width/depth/thickness of the depletion layer x_{dT} is roughly the depth that the electric field E penetrates into the p type substrate.
- Electrons make it through the depletion layer and accumulate near the semiconductor-oxide boundary, forming what is called an **inversion layer**, and, by definition, the semiconductor substrate is **n type** in the region where $E_F > E_{Fi}$!

A similar phenomenon occurs w/ an **n type substrate** (voltages & charges reversed).

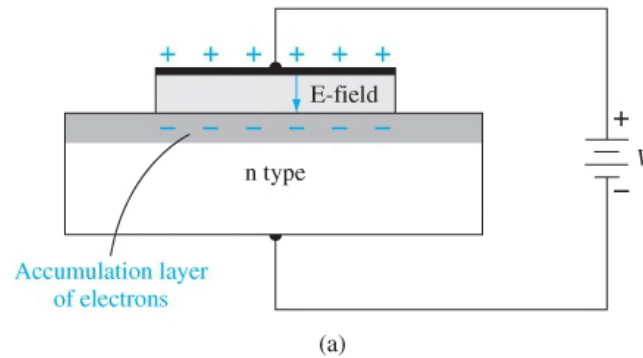


Figure 10.6 | The MOS capacitor with an n-type substrate for (a) a positive gate bias

- A **MOS capacitor** with an n type semiconductor substrate is shown above in Fig. 10.6a. The voltage source (positive at gate) moves positive charges to the top plate and electrons (negative charges) from the n type semiconductor substrate toward the bottom boundary of the oxide layer (**accumulation layer**).
- At steady-state, there is a linear relationship between positive stored charge Q and applied voltage V given by $Q = CV$.
- Here, $C = \epsilon_{\text{ox}} A / t_{\text{ox}}$ (F) and the electric field in the oxide is $E = V / t_{\text{ox}}$ (V/m or V/cm). [As before, $E \sim 0$ in the n type substrate.]
- On a per-unit-area basis, we have $C' = \epsilon_{\text{ox}} / t_{\text{ox}}$ (F/m² or F/cm²) and $Q' = C'V$ (C/m² or C/cm²).

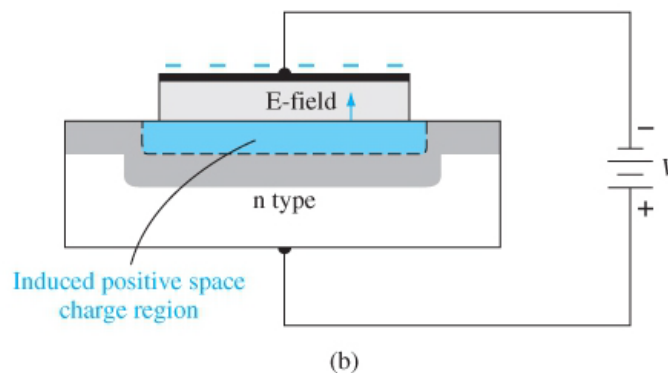


Figure 10.6 | The MOS capacitor with an n-type substrate for (b) a moderate negative gate bias.

- However, when a negative voltage is applied to the gate as shown in Fig. 10.6b, the voltage source moves negative charges to the top plate/**gate**. The electrons (negative charges) in the n type semiconductor substrate will move away from the bottom boundary of the oxide layer forming an **induced space charge region** or **depletion layer** w/ N_d^+ ions (not like a parallel plate capacitor).

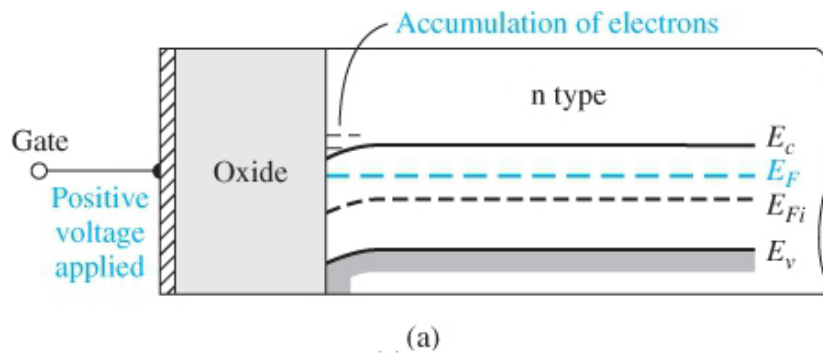


Figure 10.7 | The energy-band diagram of the MOS capacitor with an n-type substrate for (a) a positive gate bias,

- With a **positive voltage** applied at the gate (Fig. 10.7a), there is an accumulation layer of electrons near the oxide to n type semiconductor substrate boundary. This region is more strongly ‘n type’ than the rest of the substrate.
- Therefore, E_F (remains flat) must be closer to E_c than before. This results in E_c , E_v , and E_{Fi} bending down near the boundary (while maintaining their spacing).

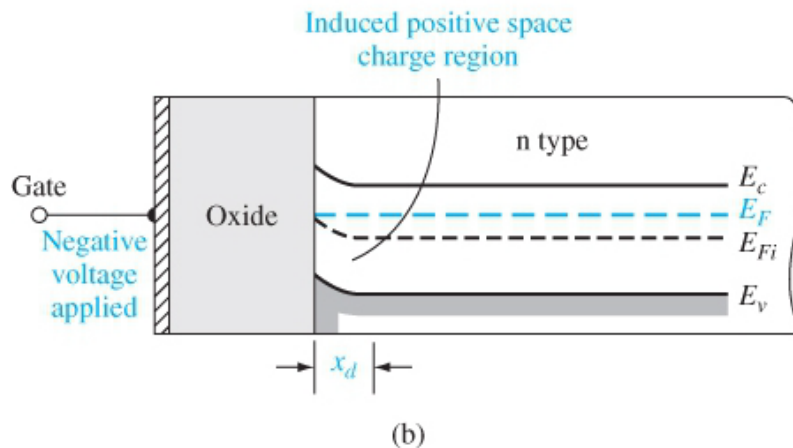


Figure 10.7 | The energy-band diagram of the MOS capacitor with an n-type substrate for (b) a moderate negative bias

- With a **negative voltage** applied at the gate (Fig. 10.7b), there is a depletion layer (w/ N_d^+ ions) near the oxide to n type substrate boundary. This region, with fewer electrons, is less ‘n type’ than the rest of the substrate.
- Therefore, E_F (remains flat) must be further from E_c than before. This results in E_c , E_v , and E_{Fi} bending up near the boundary (while maintaining their spacing).
- The width/depth/thickness of the depletion layer x_d is roughly the depth that the electric field E now penetrates into the n type substrate.

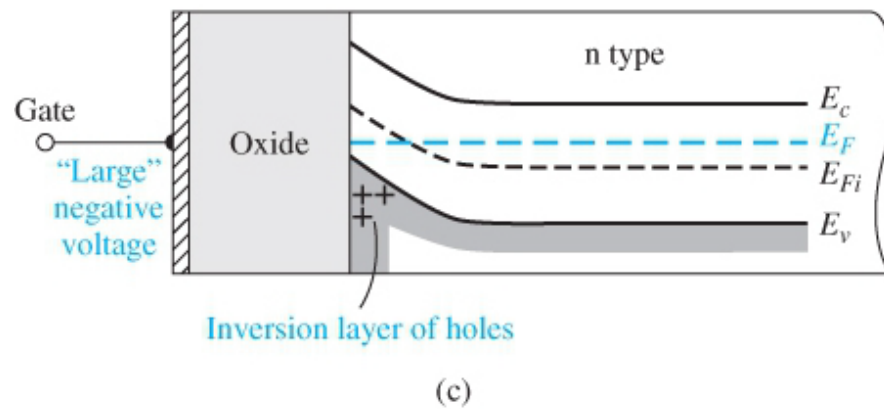


Figure 10.7 | The energy-band diagram of the MOS capacitor with an n-type substrate for (c) a “large” negative gate bias.

- When a ‘large’ negative voltage applied at the gate (Fig. 10.7c), there is a maximally thick depletion layer near the oxide to n type substrate boundary.
- Again, E_F (remains flat) is even further from E_c than before. This results in E_c , E_v , and E_{Fi} bending up near the boundary (while maintaining their spacing).
- In addition, $E_F < E_{Fi}$ and E_F gets closer to E_v than E_c near the boundary. E_F remains closer to E_c in the bulk n type substrate away from boundary.
- The width/depth/thickness of the depletion layer x_{dT} is roughly the depth that the electric field E penetrates into the n type substrate.
- Enough holes now make it through the depletion layer to accumulate near the boundary, forming what is called an **inversion layer**, and, by definition, the semiconductor substrate is **p type** in the region where $E_F < E_{Fi}$!

10.1.2 Depletion Layer Thickness

- We are now going to define some potentials (AKA voltages) in terms of energy levels (remember voltage = work / charge) in order to find the depletion layer thickness.

From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.

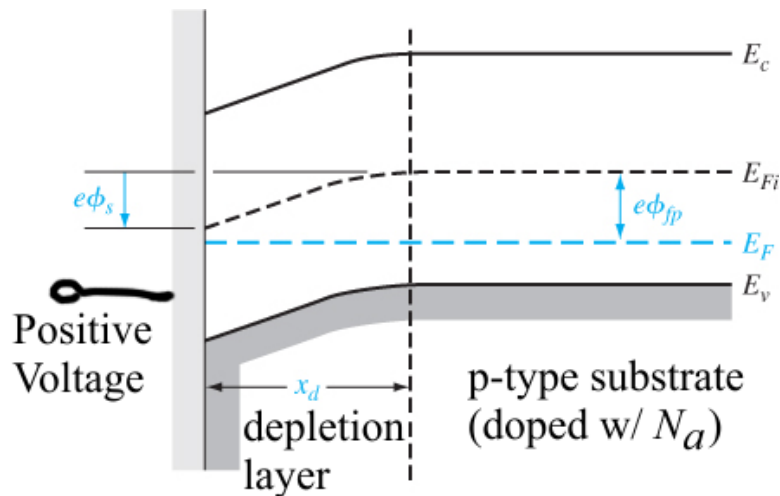


Figure 10.8 | The energy-band diagram in the p-type semiconductor, indicating surface potential.

- As shown in Figure 10.8 (above), we will define the potential ϕ_{fp} (V) associated with the energy level difference between the intrinsic Fermi energy level E_{Fi} and the Fermi energy level E_F as $E_{Fi} - E_F = e \phi_{fp}$ yielding

$$\phi_{fp} = \frac{E_{Fi} - E_F}{e} = V_t \ln\left(\frac{N_a}{n_i}\right) \quad (10.4).$$

- As shown in Figure 10.8 (above), we will define a ‘surface potential’ ϕ_s (V) associated with the change in the intrinsic Fermi energy level E_{Fi} from the bulk p-type substrate to the surface or interface with the oxide where E_{Fi} has decreased $\phi_s = \Delta E_{Fi} / e$.

- Following work in Section 7.3.3 for one-sided pn junctions, we can write

$$x_d = \left(\frac{2\epsilon_s \phi_s}{e N_a}\right)^{1/2} \quad (10.5) \text{ for p-type, or } x_d = \left(\frac{2\epsilon_s \phi_s}{e N_d}\right)^{1/2} \text{ for n-type.}$$

What happens when the applied voltage is increased to create an inversion layer? I.e., How much voltage is required? How thick is the depletion layer?

From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.

p type MOS

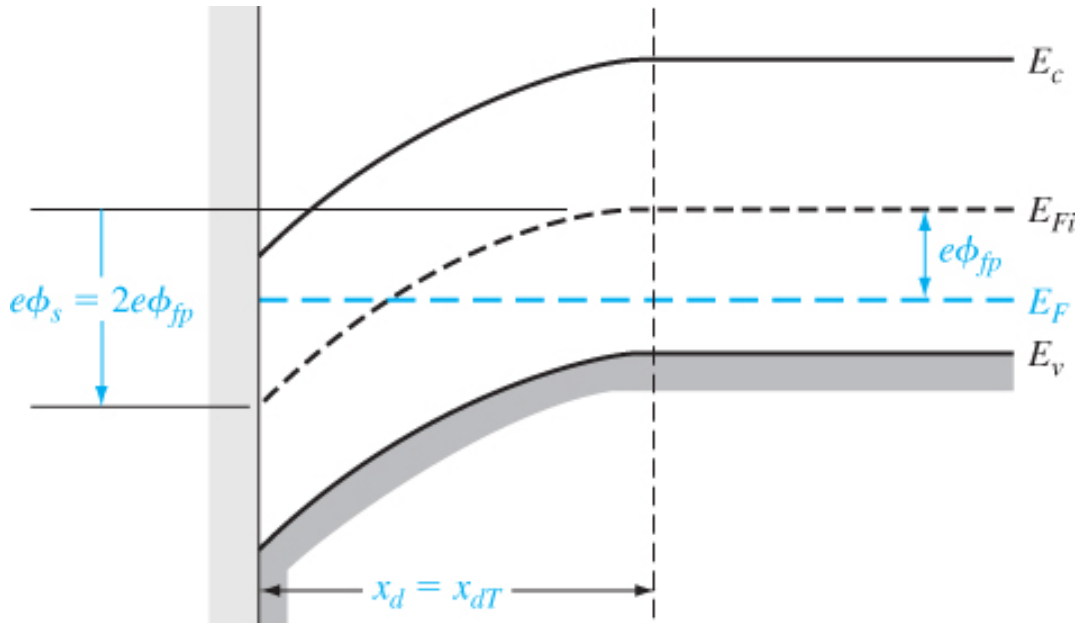


Figure 10.9 | The energy-band diagram in the p-type semiconductor at the threshold inversion point.

- We choose to define the surface inversion as “The point at which the surface is as much n type as the bulk material is p type.” This is called the **threshold inversion point**.
- This means E_{Fi} must be as much below E_F at the surface (boundary between the semiconductor and oxide) as it is above E_F in the bulk semiconductor substrate. For energy levels expressed in terms of these potentials, $e\phi_s = 2e\phi_{fp}$ at the threshold inversion point.
- This implies that the surface potential $\phi_s = 2\phi_{fp}$ (called the **threshold surface potential**) where $\phi_{fp} = V_t \ln(N_a / n_i)$ (10.4).
- Here, the depletion layer depth/thickness is $x_{dT} = \left(\frac{4\epsilon_s \phi_{fp}}{eN_a} \right)^{1/2}$ (10.6). It does not change much with increasing ϕ_s beyond the threshold voltage.

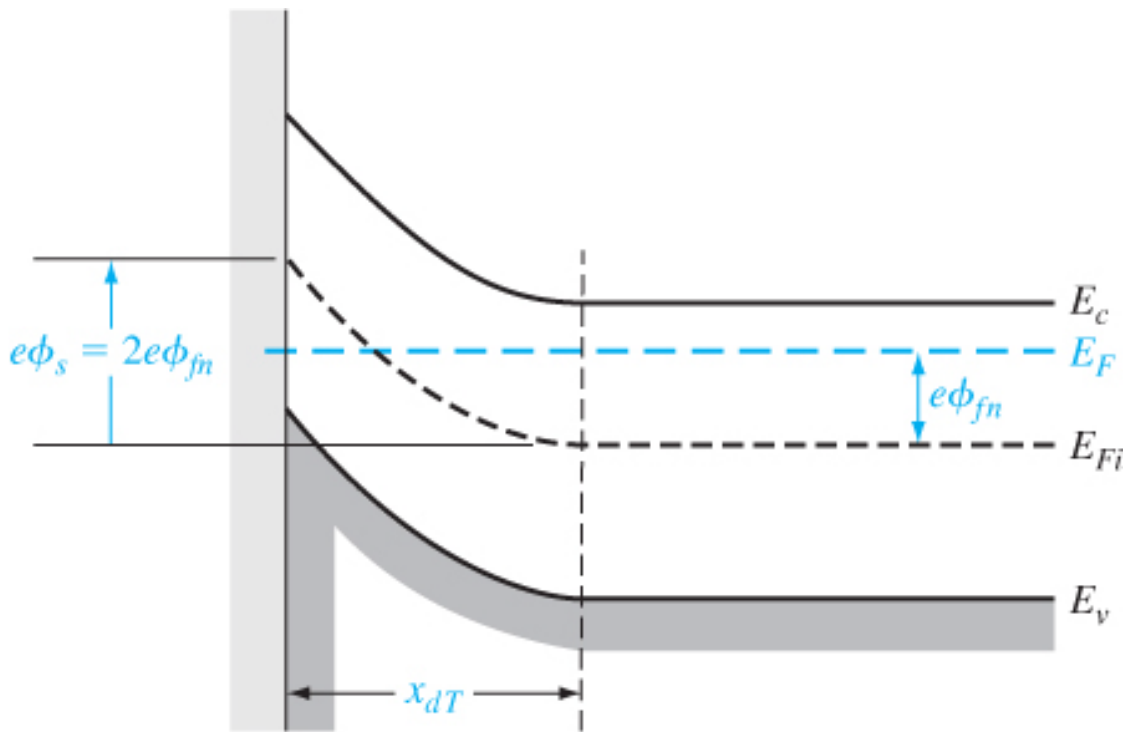
n type MOS

Figure 10.10 | The energy-band diagram in the n-type semiconductor at the threshold inversion point.

- We choose to define the surface inversion as “The point at which the surface is as much p type as the bulk material is n type.”
- This means E_{Fi} must be as much above E_F at the surface (boundary between the semiconductor and oxide) as it is below E_F in the bulk n type substrate.

➤ In terms of energy, $e\phi_s = 2e\phi_{fn}$.

➤ This implies that the surface potential $\phi_s = 2\phi_{fn}$ where

$$\phi_{fn} = V_t \ln(N_d / n_i) \quad (10.7).$$

➤ Here, the depletion layer depth/thickness is

$$x_{dT} = \left(\frac{4\epsilon_s \phi_{fn}}{e N_d} \right)^{1/2} \quad (10.8).$$

Threshold Point (p-type substrate)

- One might assume that the threshold would occur as soon as surface potential $\phi_s = \phi_{fp}$, because the concentration of majority carriers has been reduced to that of an intrinsic semiconductor at that point.
- However, as ϕ_s increases, the retreating holes “uncover” the negatively charged dopant ions N_a^- in the crystal lattice of the p-type substrate at the boundary. (These fixed ions repel the electrons needed to produce a current between the source and drain when we get to the MOSFET.)
- When ϕ_s is increased to $2\phi_{fp}$, the dopant ions are completely uncovered, such that further increases in the gate-source voltage causes electrons to flood into the channel instead of making significant increases in band bending.
- In other words, an n-layer starts to form when $\phi_s = \phi_{fp}$, but moving charges don't happen until $\phi_s = 2\phi_{fp}$.

Example- Find the potential ϕ_{fn} and depletion layer depth x_d when $\phi_s = \phi_{fn}$ for a germanium substrate doped to $N_d = 10^{15} \text{ cm}^{-3} = 10^{21} \text{ m}^{-3}$ at 300 K. Also, find the threshold surface potential and depth.

From Table B.4- $n_i = 2.4 \times 10^{13} \text{ cm}^{-3}$ and $\epsilon_s = 16\epsilon_0$.

Used donor dopants (N_d) \Rightarrow **n-type substrate!**

$$\text{Per (7.10), } V_t = \frac{k_B T}{e} = \frac{8.617333 \times 10^{-5} \text{ eV/K (300 K)}}{e} \Rightarrow \underline{V_t = 0.025852 \text{ V.}}$$

$$\text{Per (10.7), } \phi_{fn} = V_t \ln\left(\frac{N_d}{n_i}\right) = 0.025852 \ln\left(\frac{10^{15}}{2.4 \times 10^{13}}\right) \Rightarrow \underline{\phi_{fn} = 0.09642 \text{ V.}}$$

Adapting equation (10.5), we get

$$x_d = \sqrt{\frac{2\epsilon_s \phi_{fn}}{e N_d}} = \sqrt{\frac{2(16)8.8541878 \times 10^{-12} (0.09642)}{1.602176634 \times 10^{-19} (10^{21})}} \Rightarrow \underline{x_d = 4.13 \times 10^{-7} \text{ m.}}$$

$$\text{The threshold voltage is } \phi_s = 2\phi_{fn} = 2(0.09642) \Rightarrow \underline{\phi_s = 0.19284 \text{ V.}}$$

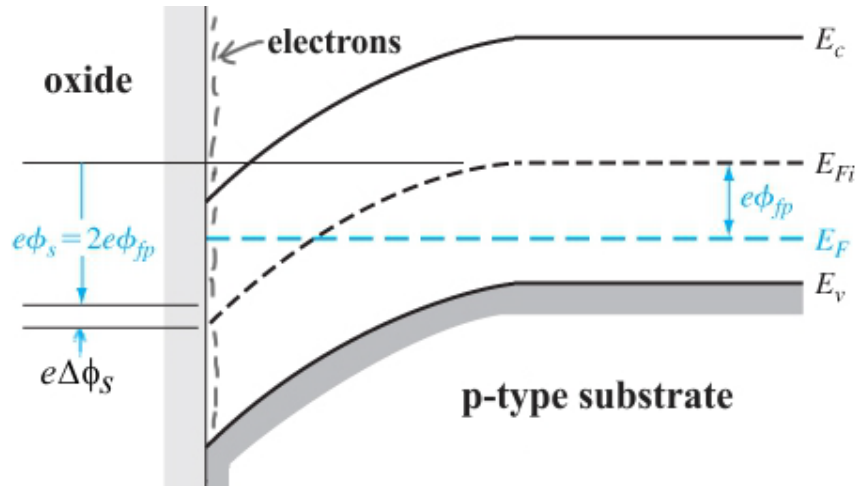
The maximum depth, per equation (10.8), is

$$x_{dT} = \sqrt{\frac{4\epsilon_s \phi_{fn}}{e N_d}} = \sqrt{\frac{4(16)8.8541878 \times 10^{-12} (0.09642)}{1.602176634 \times 10^{-19} (10^{21})}} \Rightarrow \underline{x_{dT} = 5.87 \times 10^{-7} \text{ m.}}$$

10.1.3 Surface Charge Density

- As shown below, assume we have an inversion layer at the oxide-substrate boundary of our p-type substrate, i.e., at the threshold voltage $\phi_s = 2\phi_{fp}$ plus a bit extra $\Delta\phi_s$.

From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.



What is the electron concentration in the inversion layer?

From (4.39), $n = n_i e^{(E_F - E_{Fi})/k_B T}$. Using the potentials from the picture, we can adapt this equation to get the surface charge concentration (#/cm³)

$$n_s = n_i e^{e(\phi_{fp} + \Delta\phi_s)/k_B T} = n_i e^{(\phi_{fp} + \Delta\phi_s)/V_t} = n_i e^{\phi_{fp}/V_t} e^{\Delta\phi_s/V_t} \quad (10.10a \ \& \ b).$$

Define the surface charge concentration (#/cm³) at the threshold potential as

$$\underline{n_{st} = n_i e^{\phi_{fp}/V_t}} \quad (10.11).$$

[Note : $n_{st} = N_a$ since we are at the threshold voltage where the inversion layer is as n-type as the substrate is p-type.]

We can then write $\underline{n_s = n_{st} e^{\Delta\phi_s/V_t}}$ (10.12).

From this equation, we see that n_s will climb rapidly as we go past threshold.

For n-type substrates, we get $\underline{p_{st} = n_i e^{\phi_{fp}/V_t} = N_d}$ and $\underline{p_s = p_{st} e^{\Delta\phi_s/V_t}}$.

Example- For our prior example, find the threshold inversion hole concentration p_{st} and p_s when $\Delta\phi_s = 2V_t$.

Find the potential ϕ_{fn} and depletion layer depth x_d when $\phi_s = \phi_{fn}$ for a germanium substrate doped to $N_d = 10^{15} \text{ cm}^{-3} = 10^{21} \text{ m}^{-3}$ at 300 K. Also, find the threshold surface potential and depth.

From Table B.4- $n_i = 2.4 \times 10^{13} \text{ cm}^{-3}$ and $\epsilon_s = 16\epsilon_0$.

$$\underline{V_t = 0.025852 \text{ V.}}$$

$$\underline{\phi_{fn} = 0.09642 \text{ V.}}$$

$$\underline{\phi_s = 0.19284 \text{ V.}}$$

$$p_{st} = n_i e^{\phi_{fn}/V_t} = 2.4 \times 10^{13} e^{0.09642/0.025852} \Rightarrow \underline{p_{st} = 10^{15} \text{ cm}^{-3} = N_d.}$$

$$\Delta\phi_s = 2V_t = 2(0.025852) \Rightarrow \underline{\Delta\phi_s = 0.051704 \text{ V} = 51.704 \text{ mV.}}$$

$$p_s = p_{st} e^{\Delta\phi_s/V_t} = 10^{15} e^{2V_t/V_t} \Rightarrow \underline{p_s = 7.39 \times 10^{15} \text{ cm}^{-3}.}$$

A 740% increase at only 51.7 mV past threshold!

10.1.4 Depletion Layer Thickness

We would really like to know how much voltage needs to be applied to the gate terminal to cause the substrate to be inverted at the oxide-substrate boundary of our substrate. This is going to be a ‘journey.’

We will need to introduce and define a few new parameters-

- **metal work function** $\equiv \phi_m$. The potential (V) needed to free an electron from the metal to free space; corresponding energy is $e\phi_m$ (J or eV).
- **electron affinity** $\equiv \chi$. The potential needed to free an electron from the substrate conduction band E_c to free space; corresponding energy is $e\chi$.
- **oxide electron affinity** $\equiv \chi_i$. The potential needed to free an electron from the oxide conduction band $E_{c,ox}$ to free space; corresponding energy is $e\chi_i$. This energy is in addition to the bandgap E_g energy, i.e., energy required to raise an electron from the oxide valence band E_v to conduction band E_c .

From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.

p type metal-oxide-semiconductor (MOS) w/ each material separate

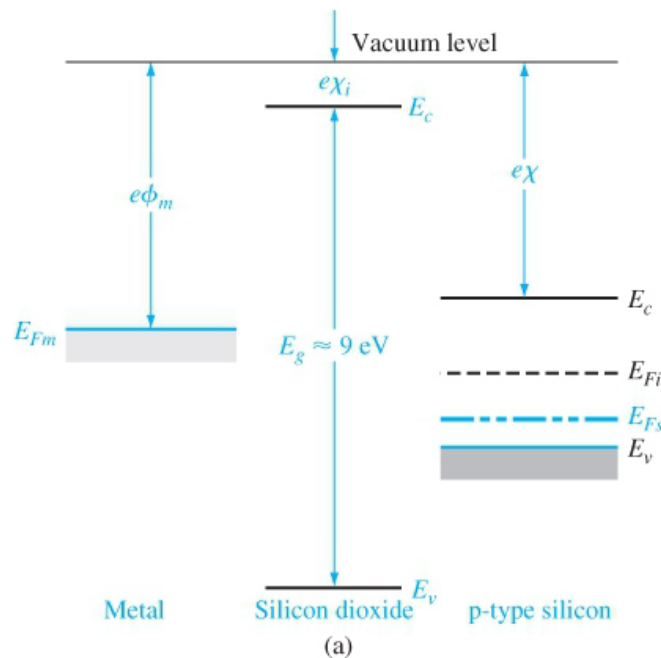


Figure 10.13 | (a) Energy levels in a MOS system prior to contact
MOS structure in thermal equilibrium after contact.

- For silicon dioxide (SiO_2), $E_g \sim 9$ eV while $e\chi_i \sim 0.9$ eV. For comparison, the bandgap energy E_g for an intrinsic silicon substrate is 1.12 eV at 300 K.

What happens when we ‘sandwich’ the metal to oxide to substrate (MOS)?

They form a ‘system.’ In a system, the Fermi energy E_F must be constant at equilibrium. In turn, this means that the energy bands in each of the materials must bend.

Now, as shown in Figure 10.13, we define -

- **modified metal work function** $\equiv \phi'_m$. The potential (V) needed to get an electron from the metal conduction band to oxide conduction band; corresponding energy is $e\phi'_m$ (J or eV).
- **modified electron affinity** $\equiv \chi'$. The potential needed to get an electron from the substrate conduction band to oxide conduction band; corresponding energy is $e\chi'$.
- **potential across oxide at zero bias** $\equiv V_{ox0}$. How much the potential changes across the oxide w/ zero applied gate voltage, due to difference in ϕ_m and χ . The energy change is eV_{ox0} .
- **surface potential at zero bias** $\equiv \phi_{s0}$. The surface potential at the oxide to substrate surface/boundary w/ zero applied gate voltage. The energy change from E_{Fi} in the bulk substrate to the surface is $e\phi_{s0}$.

p type MOS, system

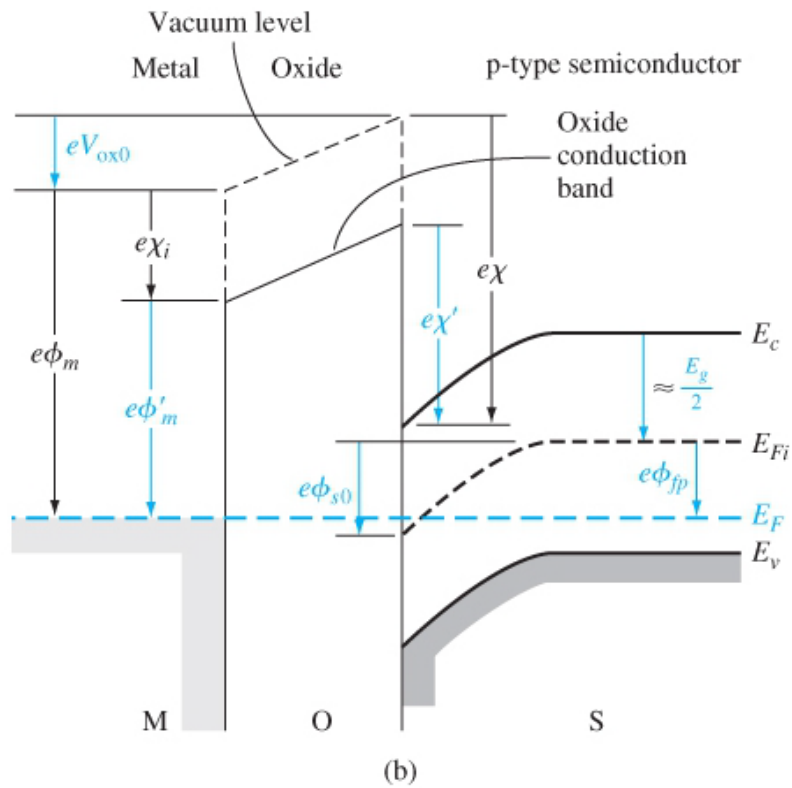


Figure 10.13 | (b) energy-band diagram through the MOS structure in thermal equilibrium after contact.

Since the Fermi energy E_F is constant for our system, we will use it as our reference. To find the voltage that must be applied to a **metal** gate to cause inversion, we will use an energy form of KVL.

- Starting at E_F in the **metal** to go up to the top of the conduction band in the oxide at the oxide-substrate surface requires $e\phi'_m + eV_{ox0}$.
- To go back down from the top of the conduction band in the oxide at the oxide-substrate surface to E_F in the bulk **substrate** will require an energy change of $e\chi' + [E_g / 2 - e\phi_{s0}] + e\phi_{fp}$.
- Equating these energies $e\phi'_m + eV_{ox0} = e\chi' + [E_g / 2 - e\phi_{s0}] + e\phi_{fp}$ (10.13).
- Rearranging yields $V_{ox0} + \phi_{s0} = -[\phi'_m - (\chi' + E_g/2e + \phi_{fp})] = -\phi_{ms}$ (10.14).
- Define a potential (V) known as the **metal-semiconductor work function difference** $\equiv \phi_{ms} = [\phi'_m - (\chi' + E_g/2e + \phi_{fp})]$ (10.15). This can be measured.

Metal to p-type Substrate ‘KVL’

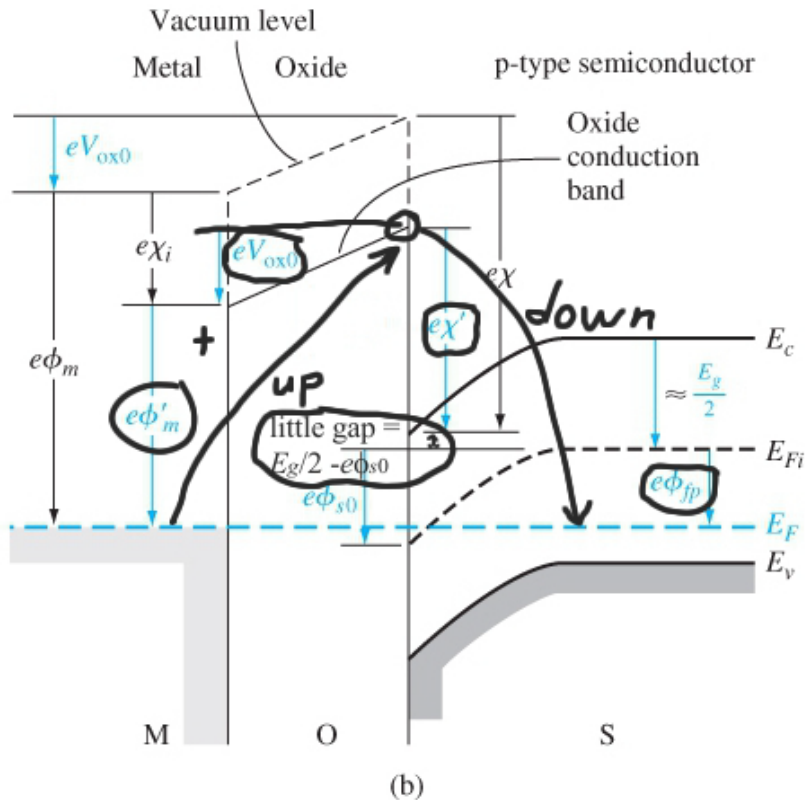


Figure 10.13 (b) energy-band diagram through the MOS structure in thermal equilibrium after contact.

To find the voltage that must be applied to a **degenerately-doped polysilicon** gate to cause inversion, we go through a similar process (see Figure 10.14).

- No metal work functions!
- For n⁺ polysilicon, we get $\phi_{ms} = -(E_g/2e + \phi_{fp})$ (10.16).
- For p⁺ polysilicon, we get $\phi_{ms} = E_g/2e - \phi_{fp}$ (10.17).

From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.

metal degenerately-doped polysilicon-oxide-semiconductor (MOS)

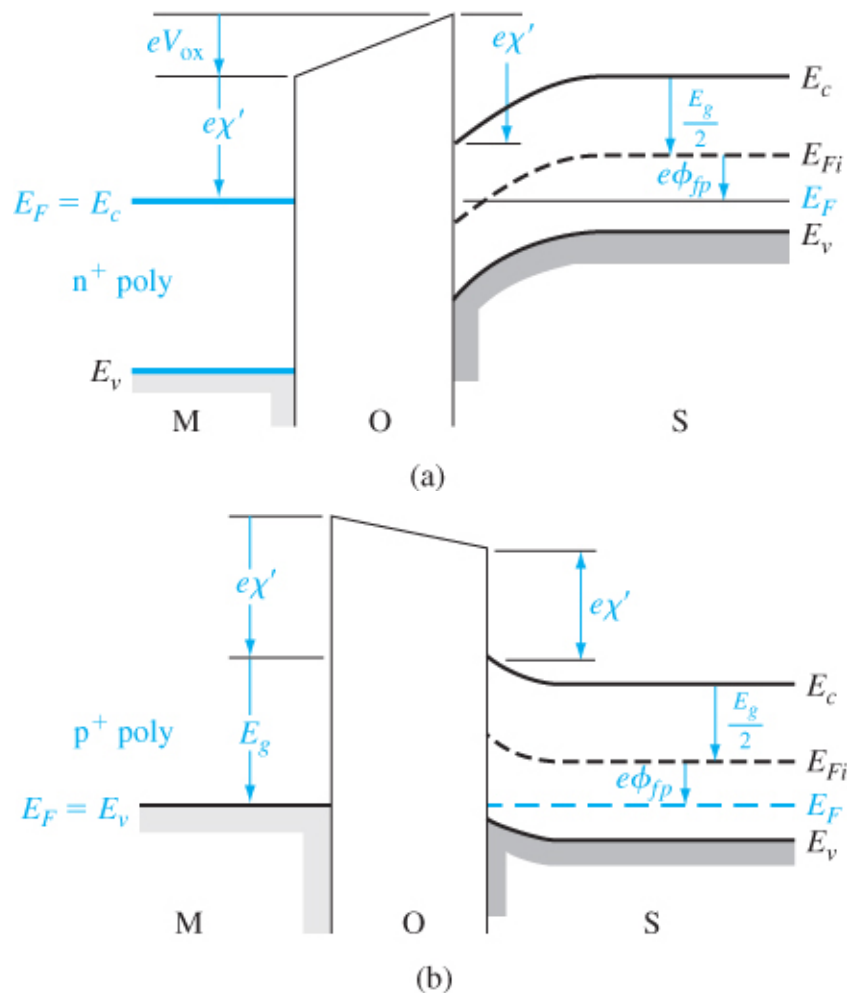


Figure 10.14 | Energy-band diagram through the MOS structure with a p-type substrate at zero gate bias for (a) an n⁺ polysilicon gate and (b) a p⁺ polysilicon gate.

What about an n-type substrate with a **metal** gate? [Note : Here the gate voltage will be **negative**.]

$$\phi_{ms} = \phi'_m - (\chi' + E_g/2e - \phi_{fp}) \quad (10.18).$$

n type semiconductor substrate MOS, system

From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.

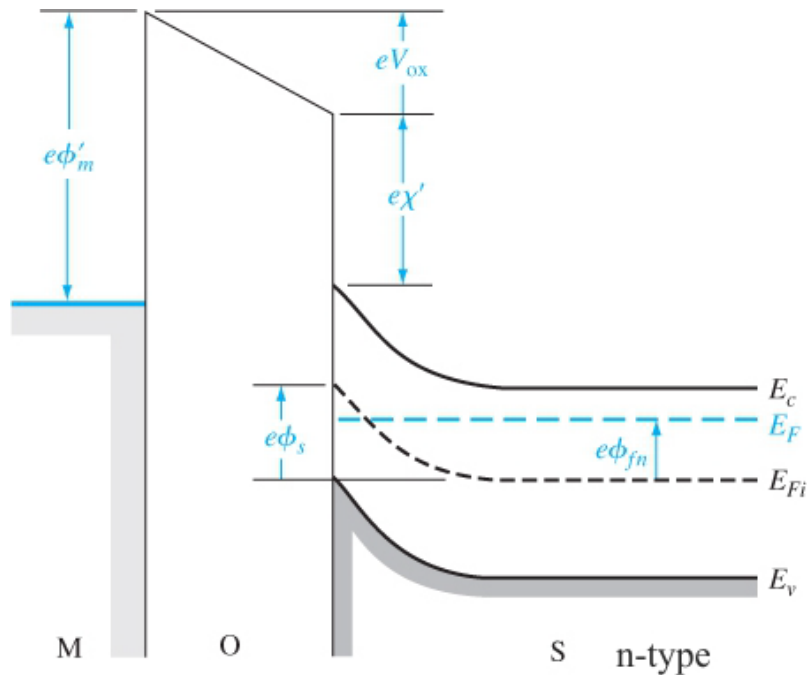


Figure 10.15 | Energy-band diagram through the MOS structure with an n-type substrate for a negative applied gate bias.

Metal-Semiconductor work function for various material and doping

From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.

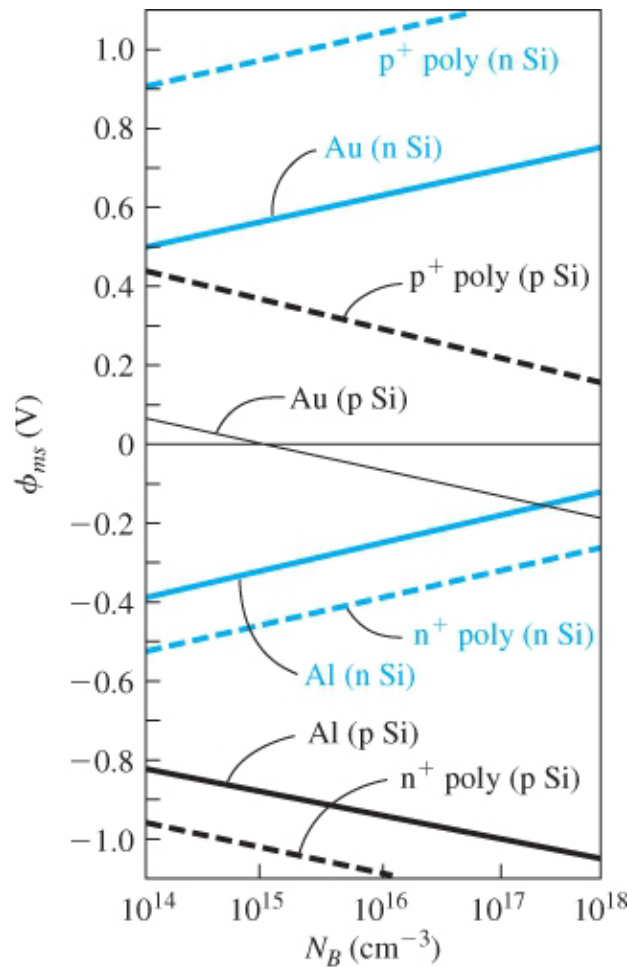


Figure 10.16 | Metal–semiconductor work function difference versus doping for aluminum, gold, and n^- and p^- polysilicon gates. (From Sze [17] and Werner [20].)

- Note, for **p-type** substrates (black lines), ϕ_{ms} decreases with increasing substrate doping concentrations.
- Note, for **n-type** substrates (blue lines), ϕ_{ms} increases with increasing substrate doping concentrations.
- ϕ_{ms} is lower (compared to metals) with degenerately-doped n^+ polysilicon used in place of metal.
- ϕ_{ms} is higher (compared to metals) with degenerately-doped p^+ polysilicon used in place of metal.

10.1.5 Flat-Band Voltage

The **flat-band voltage** is the applied voltage at the gate necessary so that the energy bands in the semiconductor substrate of the MOS are flat. This is shown in Figure 10.17 below for a p-type substrate.

From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.

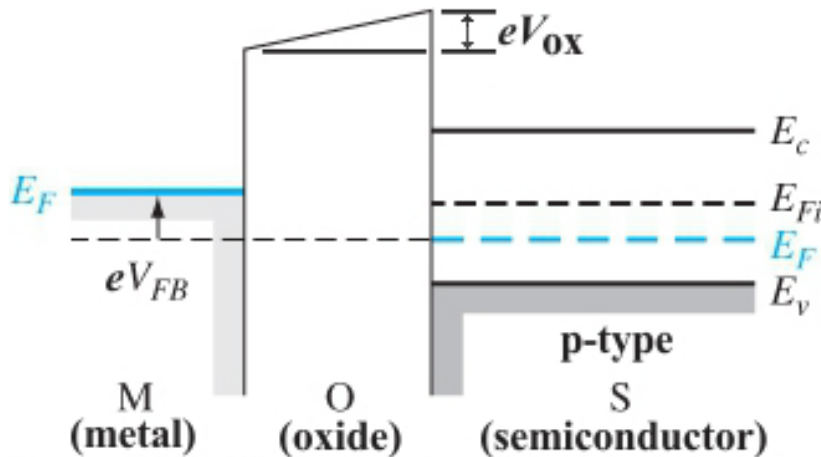


Figure 10.17 | Energy-band diagram of a MOS capacitor at flat band.

Note that there is a change in potential V_{ox} across the oxide layer. Why?

- work function difference
- Charges are usually trapped in the oxide for various reasons (until now we've assumed no trapped charges). These charges are typically positive and located near the oxide-semiconductor boundary.
- For analysis, assume these charges Q'_{ss} (traditionally $\#/m^2$ or $\#/cm^2$) are at the boundary. [Note, multiply by electron charge magnitude e to get surface charge density in C/m^2 or C/cm^2 .]
- Per (10.14) & (10.15), $V_{ox0} + \phi_{s0} = -\phi_{ms}$ (10.19) at zero bias.
- Applying a gate voltage V_G changes this to

$$V_G = \Delta V_{ox0} + \Delta \phi_s = (V_{ox} - V_{ox0}) + (\phi_s - \phi_{s0}).$$

- Using (10.19), we get $V_G = \Delta V_{ox0} + \Delta \phi_s = V_{ox} + \phi_s + \phi_{ms}$ (10.21).

- At **flat-band**, the electric field is zero ($E = 0$) in the semiconductor substrate. Therefore, the trapped charges Q'_{ss} will attract charges Q'_m to the surface of the metal adjoining the oxide as shown in Figure 10.18. By conservation of charge, $Q'_{ss} + Q'_m = 0$ or $Q'_m = -Q'_{ss}$.

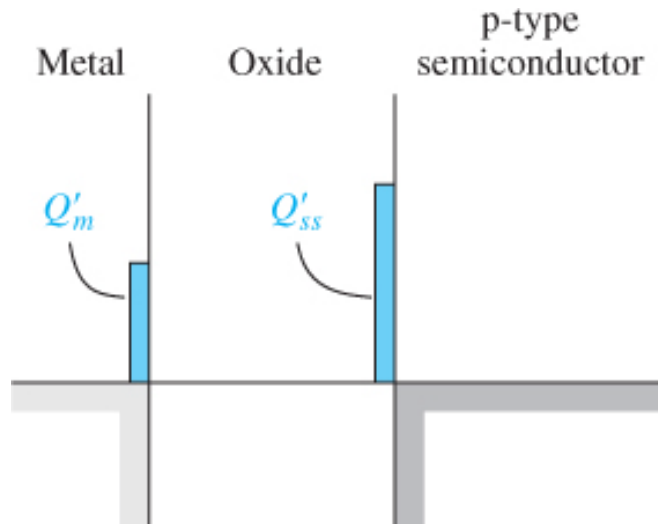


Figure 10.18 | Charge distribution in a MOS capacitor at flat band.

- A capacitance per unit area in the oxide $C_{ox} = \epsilon_{ox} / t_{ox}$ (F/m² or F/cm²) is defined per (10.1) to relate the voltage across the oxide to the charges

$$V_{ox} = Q'_m / C_{ox} \quad (10.23) \quad \text{or} \quad V_{ox} = -Q'_{ss} / C_{ox} \quad (10.24).$$

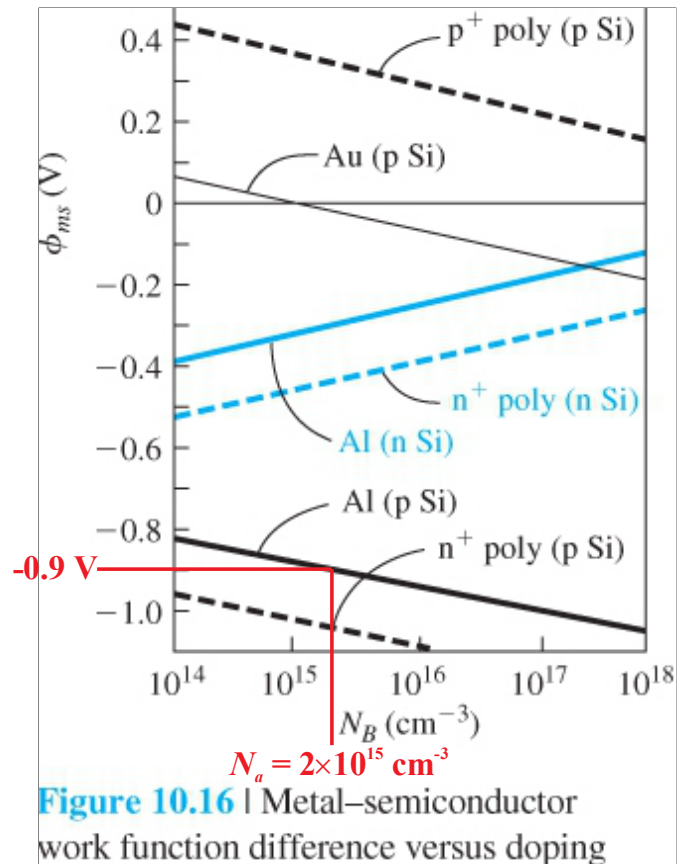
- Going back to (10.21) and noting that $\phi_s = 0$ at flat-band, we get our flat-band gate voltage to be

$$V_G = \boxed{V_{FB} = V_{ox} + \phi_{ms} = \phi_{ms} - Q'_{ss} / C_{ox}} \quad (10.25).$$

Example- Find the flat-band voltage for a p-type silicon substrate MOS with $N_a = 2 \times 10^{15} \text{ cm}^{-3}$ at 300 K. The oxide (SiO_2) layer is 60 nm thick with a trapped charge concentration of $4 \times 10^{10} \text{ \#/cm}^2$. The gate is made of aluminum.

From Table B.6- $\epsilon_{\text{ox}} = 3.9\epsilon_0$.

From Figure 10.16- $\phi_{ms} = -0.9 \text{ V}$.



$$C_{\text{ox}} = \epsilon_{\text{ox}}/t_{\text{ox}} = 3.9(8.8542 \times 10^{-12})/60 \times 10^{-9}$$

$$\Rightarrow \underline{C_{\text{ox}} = 5.755 \times 10^{-4} \text{ (F/m}^2\text{)} = 5.755 \times 10^{-8} \text{ (F/cm}^2\text{)}}.$$

$$Q'_{ss} = e (4 \times 10^{10} \text{ \#/cm}^2) = 1.602176634 \times 10^{-19} (4 \times 10^{10})$$

$$\Rightarrow \underline{Q'_{ss} = 6.4087 \times 10^{-9} \text{ (C/cm}^2\text{)}}.$$

$$\text{Per (10.22), } V_{FB} = \phi_{ms} - Q'_{ss} / C_{\text{ox}} = -0.9 - 6.4087 \times 10^{-9} / 5.755 \times 10^{-8}$$

$$\Rightarrow \underline{V_{FB} = -1.015 \text{ (V)}}.$$

10.1.6 Threshold Voltage

The **threshold voltage** V_T is the applied voltage at the gate necessary so that an inversion layer is established at the surface of the semiconductor substrate adjoining the oxide.

➤ Earlier, we defined that $\phi_s = 2\phi_{fp}$ for inversion. Therefore, $V_T > V_{FB}$.

From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.

p-type metal-oxide-semiconductor (MOS) at threshold voltage

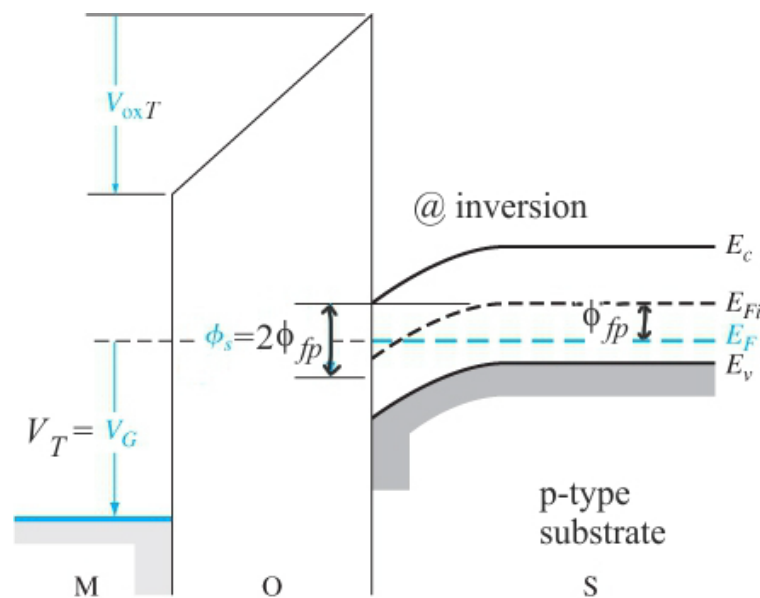


Figure 10.20 | Energy-band diagram through the MOS structure with a positive applied gate bias.

- Set gate voltage to achieve inversion of substrate, i.e., $V_G = V_T$.
- Note, E_{Fi} in substrate is bent so that surface potential is $\phi_s = 2\phi_{fp}$.
- Therefore, there is a depletion layer of thickness x_{dT} containing the ionized dopant atoms; N_a^- for a p-type substrate and N_d^+ for an n-type substrate.
- Now, we have changes in the surface charge densities at the metal-oxide interface and on the semiconductor side of the oxide-semiconductor boundary as shown in Figure 10.19.

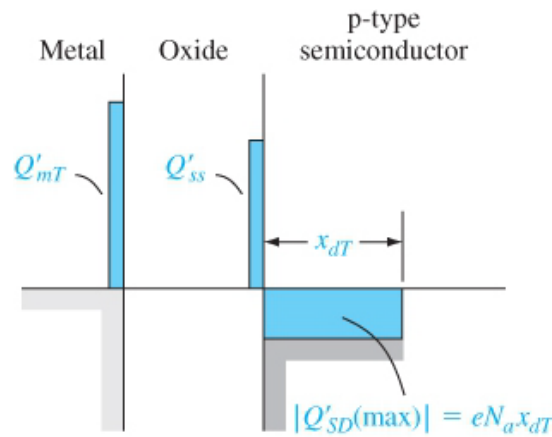


Figure 10.19 | Charge distribution in a MOS capacitor with a p-type substrate at the threshold inversion point.

- $Q'_{mT} \equiv$ charge density (C/m^2) build-up on the metal gate at threshold.
- The charge density in the depletion layer at threshold $|Q'_{SD(max)}|$.
- By conservation of charge,

$$Q'_{ss} + Q'_{mT} = |Q'_{SD(max)}| = e N_a x_{dT} \quad (10.26 \ \& \ 10.27).$$

- Going back to (10.21) and noting that $\phi_s = 0$ at flat-band, we get our threshold gate voltage V_{TN} (T for threshold & N for electrons in inversion layer) to be

$$V_G = \boxed{V_{TN} = V_{oxT} + 2\phi_{fp} + \phi_{ms}} \quad (10.28).$$

where V_{oxT} is the voltage across the oxide layer at threshold.

- V_{oxT} can be put in terms of the oxide capacitance and the charges as

$$V_{oxT} = Q'_{mT} / C_{ox} = (-Q'_{ss} + |Q'_{SD(max)}|) / C_{ox} \quad (10.30).$$

- Now, the threshold gate voltage can be written

$$\boxed{V_{TN} = \frac{|Q'_{SD(max)}|}{C_{ox}} - \frac{Q'_{ss}}{C_{ox}} + \phi_{ms} + 2\phi_{fp}} \quad (10.31a)$$

or

$$\boxed{V_{TN} = \frac{|Q'_{SD(max)}|}{C_{ox}} + V_{FB} + 2\phi_{fp}} \quad (10.31c).$$

- For a p-type substrate, $V_{TN} < 0$ implies a depletion mode device (i.e., inversion layer w/ no applied gate voltage) whereas $V_{TN} > 0$ is an enhancement mode device.

What about n-type substrates?

From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.

n-type metal-oxide-semiconductor (MOS)

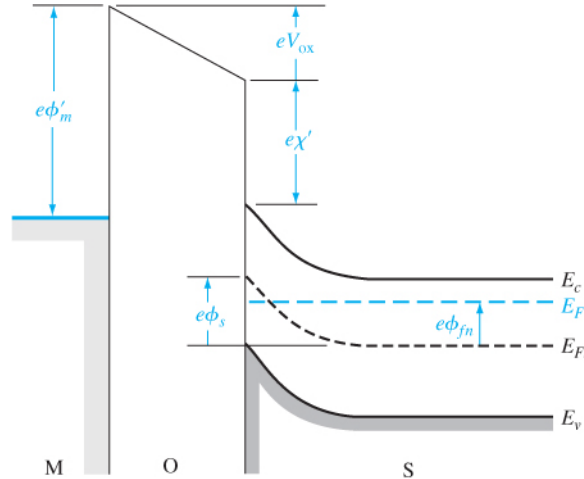


Figure 10.15 | Energy-band diagram through the MOS structure with an n-type substrate for a negative applied gate bias.

- Following a similar process, we get our threshold gate voltage V_{TP} (T for threshold & P for holes in version layer) to be

$$V_{TP} = \frac{-|Q'_{SD}(\max)|}{C_{ox}} - \frac{Q'_{ss}}{C_{ox}} + \phi_{ms} - 2\phi_{fn} \quad (10.32)$$

where

$$\phi_{ms} = \phi'_m - (\chi' + E_g/2e - \phi_{fp}) \quad (10.18)/(10.33a),$$

$$|Q'_{SD}(\max)| = e N_d x_{dT} \quad (10.33b),$$

$$x_{dT} = \left(\frac{4\epsilon_s \phi_{fn}}{e N_d} \right)^{1/2} \quad (10.8)/(10.33c), \text{ and}$$

$$\phi_{fn} = V_t \ln(N_d / n_i) \quad (10.7)/(10.33d).$$

Note: The flat-band voltage is still $V_{FB} = \phi_{ms} - Q'_{ss} / C_{ox}$ (10.25).

Example- Find the threshold voltage (& related quantities) for a MOS capacitor at 300 K with a gold metal gate. It has silicon dioxide for the oxide layer of thickness 21 nm with an equivalent trapped charge density of $2 \times 10^{11} \text{ cm}^{-2}$ and a p-type silicon substrate where $N_a = 10^{17} \text{ cm}^{-3}$.

Tables B.4 & B.6- $n_i = 1.5 \times 10^{10} \text{ cm}^{-3}$, $\epsilon_{\text{Si}} = 11.7\epsilon_0$, and $\epsilon_{\text{SiO}_2} = 3.9\epsilon_0$ at 300 K.

Oxide capacitance per unit area is (10.1) $C' = \epsilon/d \Rightarrow C_{ox} = \epsilon_{ox}/t_{ox}$

$$C_{ox} = 3.9(8.8541878 \times 10^{-12} \text{ F/m}) / 21 \times 10^{-9} \text{ m}$$

$$\Rightarrow \underline{C_{ox} = 1.64435 \times 10^{-3} \text{ F/m}^2 = 1.64435 \times 10^{-7} \text{ F/cm}^2}.$$

Equivalent trapped charge density is

$$Q'_{ss} = 1.6021766 \times 10^{-19} \text{ C} (2 \times 10^{11} \text{ cm}^{-2}) \Rightarrow \underline{Q'_{ss} = 3.204353 \times 10^{-8} \text{ C/cm}^2}.$$

From Figure 10.16, the metal-semiconductor work function for gold to p-type silicon semiconductor substrate is $\Rightarrow \underline{\phi_{ms} = -0.13 \text{ V}}$.

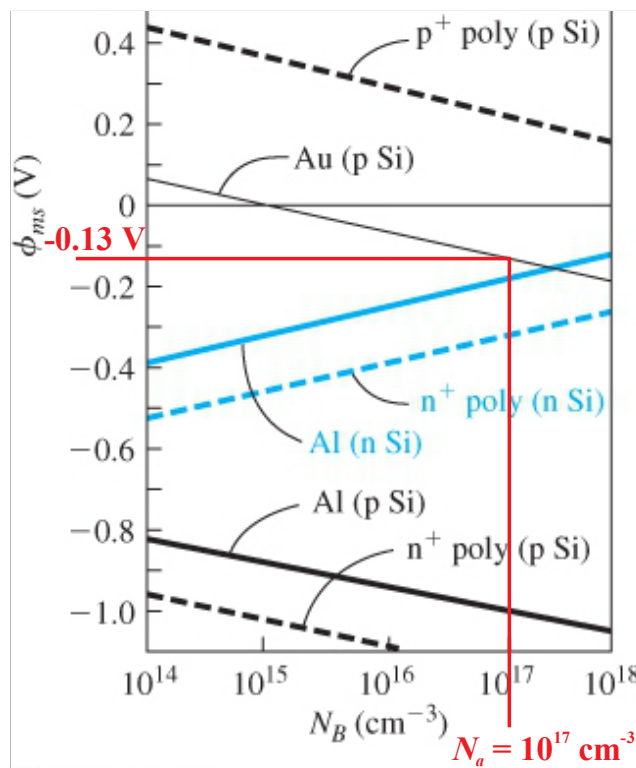


Figure 10.16 | Metal-semiconductor work function difference versus doping

From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.

Per (10.25), the flat-band voltage is-

$$V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}} = -0.13 - \frac{3.20435 \cdot 10^{-8}}{1.64435 \cdot 10^{-7}} = -0.13 - 0.19487 \Rightarrow \underline{V_{FB} = -0.32487 \text{ V.}}$$

Per (10.4), the potential difference between E_{Fi} and E_F in the substrate is

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = 0.025852 \ln\left(\frac{10^{17}}{1.5 \cdot 10^{10}}\right) \Rightarrow \underline{\phi_{fp} = 0.406203 \text{ V.}}$$

Per (10.6), the maximum depletion layer width (use MKS units) is

$$x_{dT} = \left(\frac{4 \epsilon_s \phi_{fp}}{e N_a}\right)^{1/2} = \sqrt{\frac{4(11.7)8.8541878 \times 10^{-12} (0.406203)}{(1.602176634 \times 10^{-19})10^{23}}} \Rightarrow \underline{x_{dT} = 1.024976 \times 10^{-7} \text{ m.}}$$

Per (10.27), the maximum depletion layer charge density (use MKS units) is

$$\left|Q'_{SD}(\text{max})\right| = e N_a x_{dT} = (1.602176634 \times 10^{-19})10^{23} (1.024976 \times 10^{-7}) \Rightarrow \underline{|Q'_{SD}(\text{max})| = 1.64219 \times 10^{-3} \text{ C/m}^2 = 1.64219 \times 10^{-7} \text{ C/cm}^2.}$$

Per (10.31c), the threshold voltage (use MKS units) is

$$V_{TN} = \frac{|Q'_{SD}(\text{max})|}{C_{ox}} + V_{FB} + 2\phi_{fp} = \frac{1.64219 \times 10^{-3}}{1.64435 \times 10^{-3}} + (-0.32487) + 2(0.406203) \Rightarrow \underline{V_{TN} = 1.48622 \text{ V.}}$$

(This is an enhancement mode device.)

10.2 Capacitance-Voltage Characteristics

10.2.1 Ideal C-V Characteristics

From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.

p type metal-oxide-semiconductor (MOS) capacitor

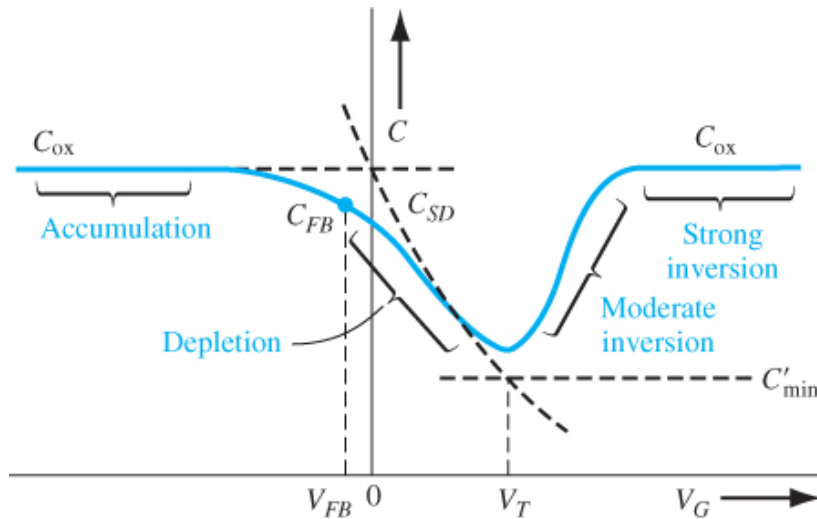


Figure 10.26 | Ideal low-frequency capacitance versus gate voltage of a MOS capacitor with a p-type substrate. Individual capacitance components are also shown.

- The capacitance goes through different modes, i.e., accumulation, depletion, moderate inversion, & strong inversion, as the gate voltage V_G increases.

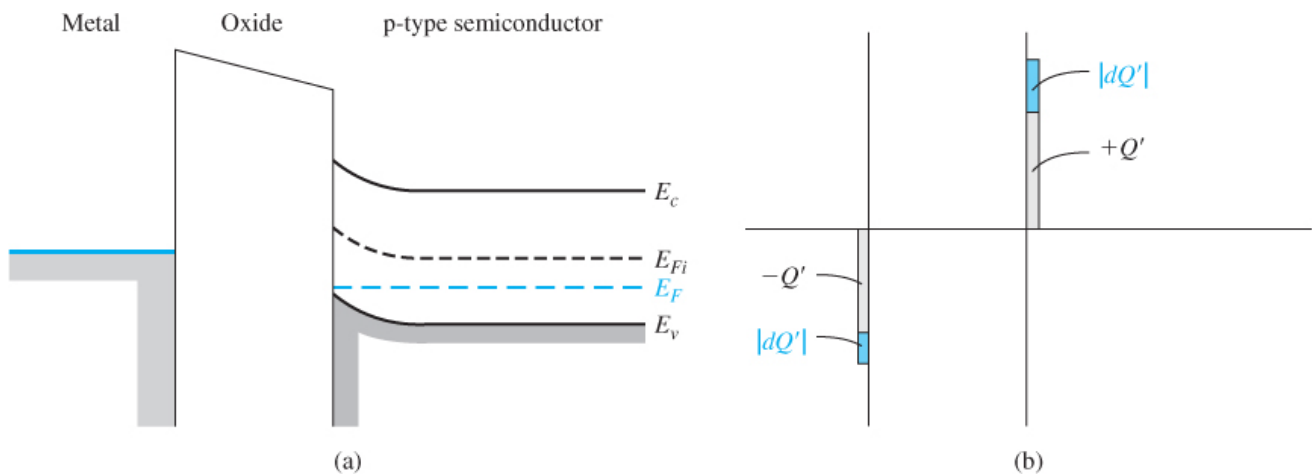


Figure 10.23 | (a) Energy-band diagram through a MOS capacitor for the accumulation mode. (b) Differential charge distribution at accumulation for a differential change in gate voltage.

- **Accumulation mode** ($V_G < 0$)
- Like parallel-plate capacitor, capacitance is constant $C_{ox} = \epsilon_{ox} / t_{ox}$ (F/m² or F/cm²)

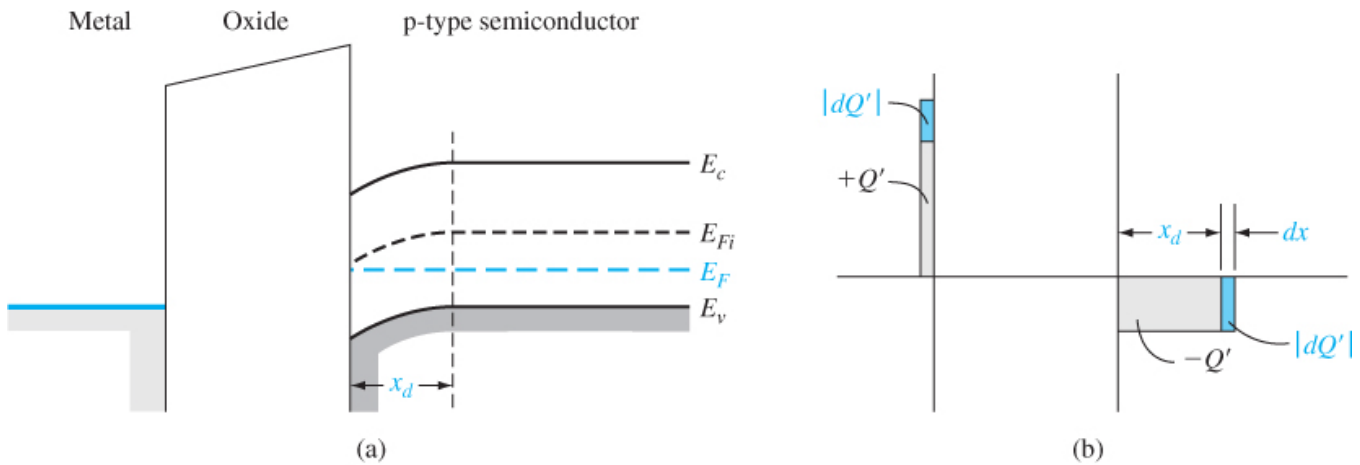


Figure 10.24 | (a) Energy-band diagram through a MOS capacitor for the depletion mode. (b) Differential charge distribution at depletion for a differential change in gate voltage.

➤ **Depletion mode** (V_G transitions from negative to positive, and depletion layer depth/thickness x_d climbs toward x_{dT})

➤ Capacitance is a combination of that from oxide and that from depletion layer charges $\frac{1}{C'(\text{depl})} = \frac{1}{C_{ox}} + \frac{1}{C_{SD}'}$ or $C'(\text{depl}) = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)x_d}$.

➤ At flat band, when $V_G = V_{FB}$, $C'_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)\sqrt{\frac{k_B T}{e} \left(\frac{\epsilon_s}{eN_a}\right)}}$.

➤ Minimum at threshold, when $V_G = V_{TG} = V_T$, $C'_{\min} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)x_{dT}}$.

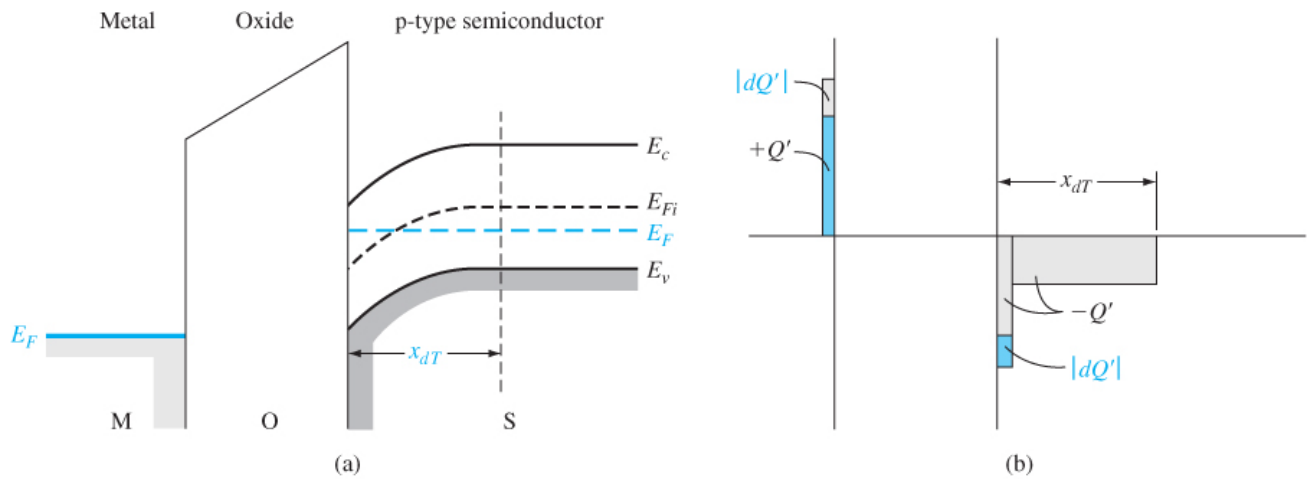


Figure 10.25 | (a) Energy-band diagram through a MOS capacitor for the inversion mode. (b) Differential charge distribution at inversion for a low-frequency differential change in gate voltage.

- Moderate and strong **inversion modes** ($V_G > V_T$ and inversion layer depth/thickness is x_{dT})
- For **moderate inversion**, capacitance begins rising toward a constant value of $C'(inv) = C_{ox} = \epsilon_{ox} / t_{ox}$ (F/m² or F/cm²) of the **strong inversion mode**, i.e., it begins acting like parallel-plate capacitor again.

n type metal-oxide-semiconductor (MOS) capacitor

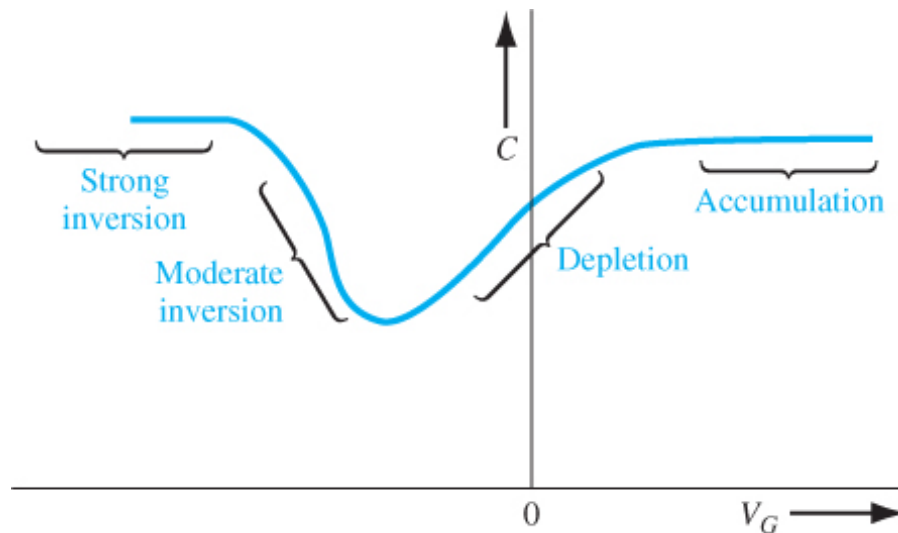


Figure 10.27 | Ideal low-frequency capacitance versus gate voltage of a MOS capacitor with an n-type substrate.

- The capacitance goes through different modes, i.e., accumulation, depletion, moderate inversion, & strong inversion, as the gate voltage **decreases**.

10.2.2 Frequency Effects, 10.2.3 Fixed Oxide and Interface Charge Effects- skip

10.3 The Basic MOSFET Operation

The MOS capacitor is turned into a MOSFET by adding two regions (called Source and Drain) to the substrate on either side of the oxide layer with doping opposite to the main body of the substrate.

10.3.1 MOSFET Structures

From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.

n-channel enhancement mode MOSFET

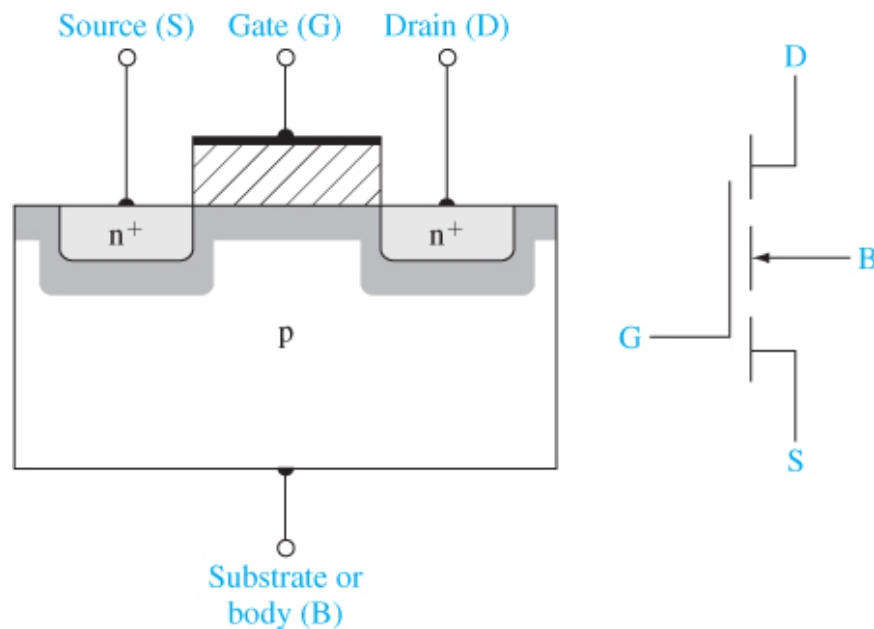


Figure 10.34 | Cross section and circuit symbol for an n-channel enhancement mode MOSFET.

- There is NOT an inversion layer when the gate voltage is zero ($V_G = 0$).
- A positive gate voltage ($V_G > 0$, e.g., $V_G \geq V_T$) induces an n-type inversion layer in the p-type substrate below the **Gate (G)** which creates a path connecting the n-type **Source (S)** and n-type **Drain (D)** for electrons to flow from source to drain, i.e., conventional current flows from D to S (opposite).
- Note: If $V_G < V_T$ there is NOT an inversion layer \Rightarrow **cutoff mode** w/ $I_D \approx 0$.
- Circuit symbol is shown to the right. Note that there are separate lines touching D, S, and the **Body (B)**. This is to indicate that there is NOT an n channel when $V_G = 0$.

n-channel depletion mode MOSFET

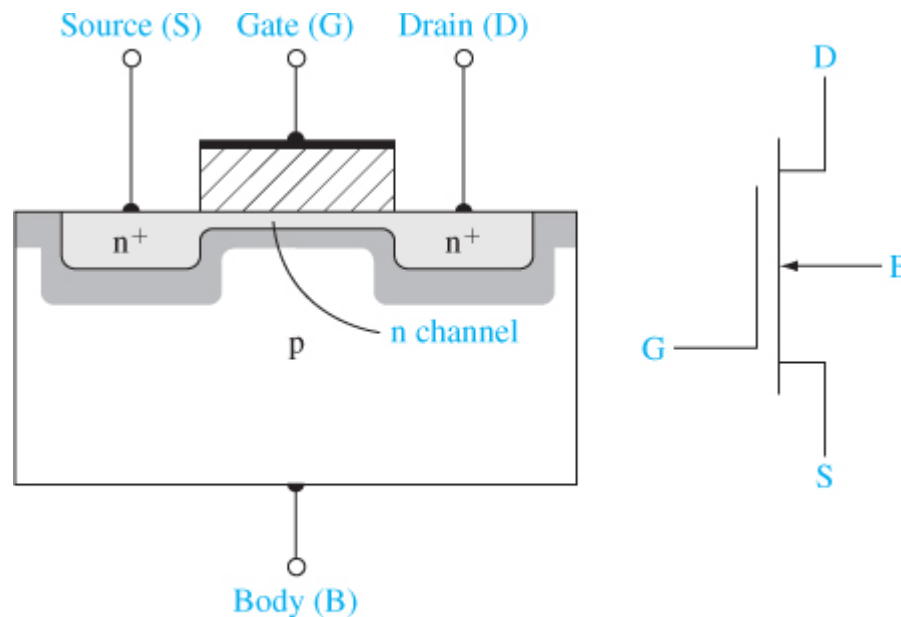


Figure 10.35 | Cross section and circuit symbol for an n-channel depletion mode MOSFET.

- There IS an inversion layer when the gate voltage is zero ($V_G = 0$).
- The n channel can be an n-type inversion layer **or** an intentionally doped n region.
- There is a path connecting the source and drain for electrons to flow from the source to the drain, i.e., conventional current flows from the drain to the source.
- Circuit symbol is shown to the right. Note that there is a single line touching D, S, and B to indicate the existence of the n channel with $V_G = 0$.

p-channel enhancement mode MOSFET

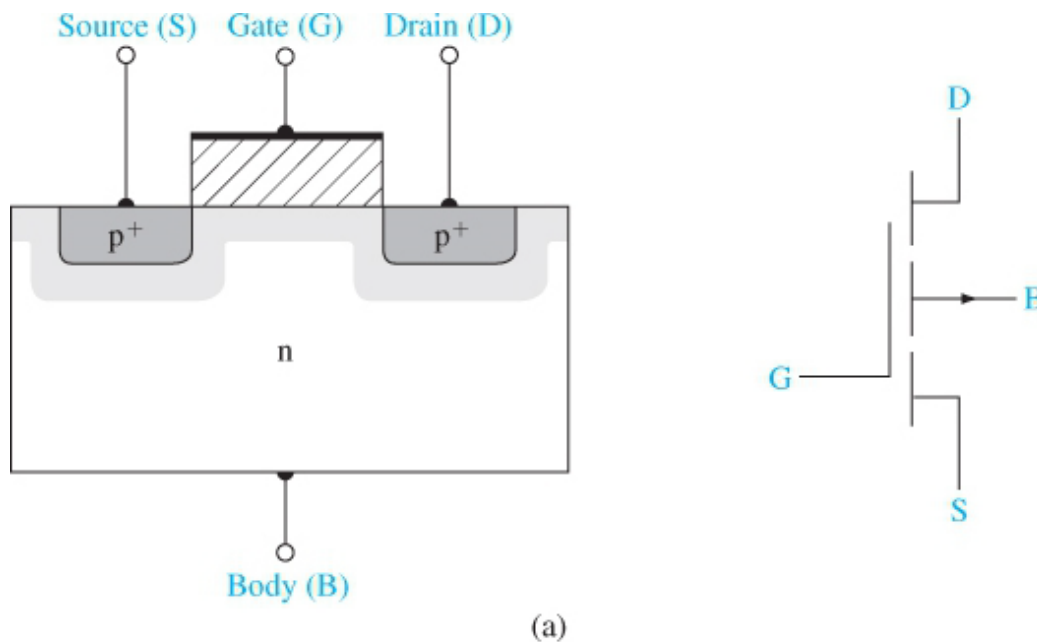


Figure 10.36 | Cross section and circuit symbol for (a) a p-channel enhancement mode MOSFET

- There is NOT an inversion layer when the gate voltage is zero ($V_G = 0$).
- A negative gate voltage ($V_G < 0$, e.g., $V_G \leq V_T$) induces an p-type inversion layer in the n-type substrate below the **Gate (G)** which creates a path connecting the p-type **Source (S)** and p-type **Drain (D)** for holes to flow from the source to the drain, i.e., conventional current flows from S to D (same).
- Note: If $V_G > V_T$ there is NOT an inversion layer \Rightarrow **cutoff mode** w/ $I_D \approx 0$.
- Circuit symbol is shown to the right. Note that there are separate lines touching D, S, and the **Body (B)**. This is to indicate that there is NOT a p channel when $V_G = 0$.

n-channel depletion mode MOSFET

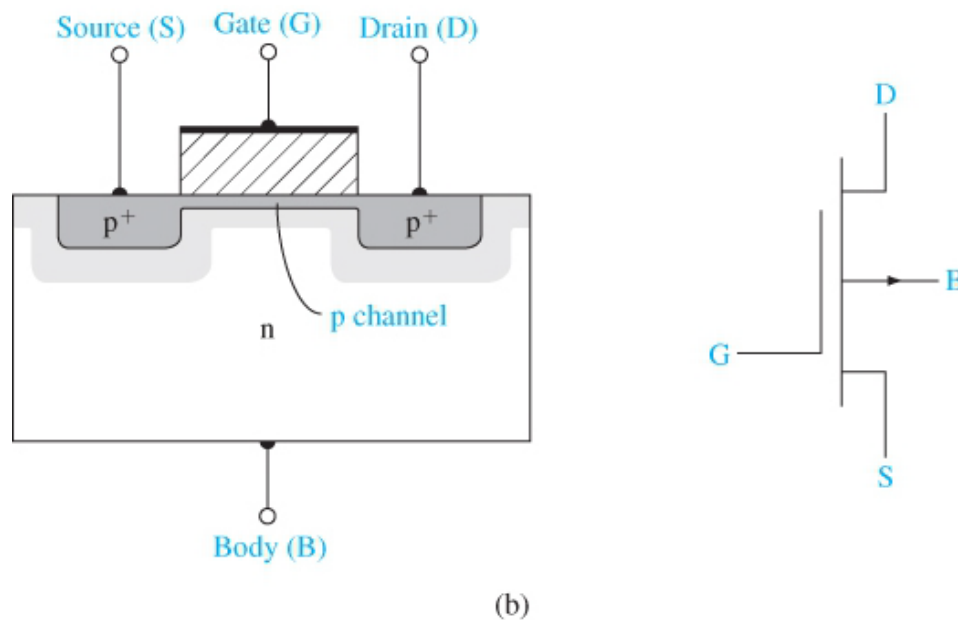


Figure 10.36 | Cross section and circuit symbol for (b) a p-channel depletion mode MOSFET.

- There IS an inversion layer when the gate voltage is zero ($V_G = 0$).
- The p channel can be an p-type inversion layer **or** an intentionally doped p region.
- There is a path connecting the source and drain for holes to flow from the source to the drain, i.e., conventional current flows from S to D (same).
- Circuit symbol is shown to the right. Note that there is a single line touching D, S, and B to indicate the existence of the p channel with $V_G = 0$.

10.3.2 Current-Voltage Relationship- Concepts

From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.

n-channel enhancement mode MOSFET

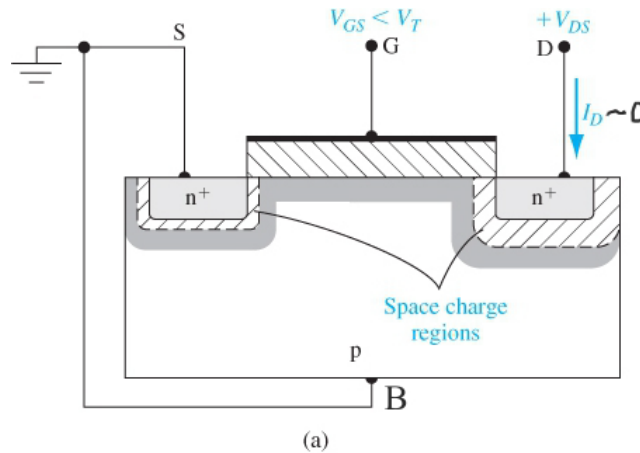


Figure 10.37 | The n-channel enhancement mode MOSFET

(a) with an applied gate voltage $V_{GS} < V_T$

- The source (S) and body (B) are tied together and grounded.
- The gate (G) voltage V_G has been renamed V_{GS} while the drain (D) voltage has been renamed V_{DS} , i.e., they are referenced to ground (node voltages).
- With $V_{GS} < V_T$, there is no inversion layer (AKA n channel). In fact, there is a depletion layer (space charge region) between the n^+ drain & source and the p-type substrate (**cutoff mode**). Therefore, $I_D \sim 0$ (ignore leakage) even with $V_{DS} > 0$.

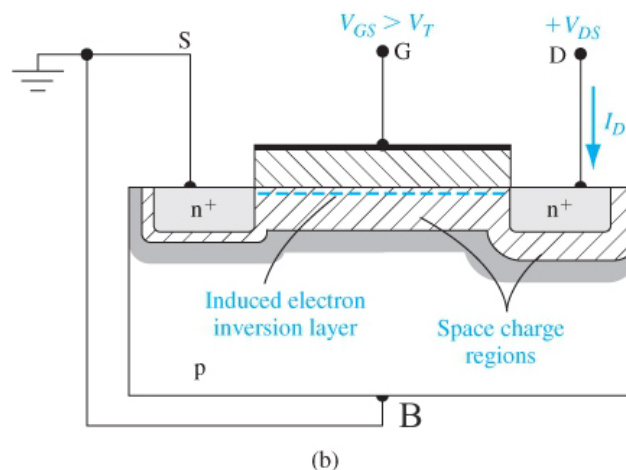


Figure 10.37 | The n-channel enhancement mode MOSFET

(b) with an applied gate voltage $V_{GS} > V_T$.

- With $V_{GS} \geq V_T$, there **IS** an inversion layer (AKA n channel). Now, $I_D > 0$ with $V_{DS} > 0$. [Reality: electrons to flow from the source to the drain.]

Reality- can't keep increasing V_{DS} with a corresponding linear increase in I_D .

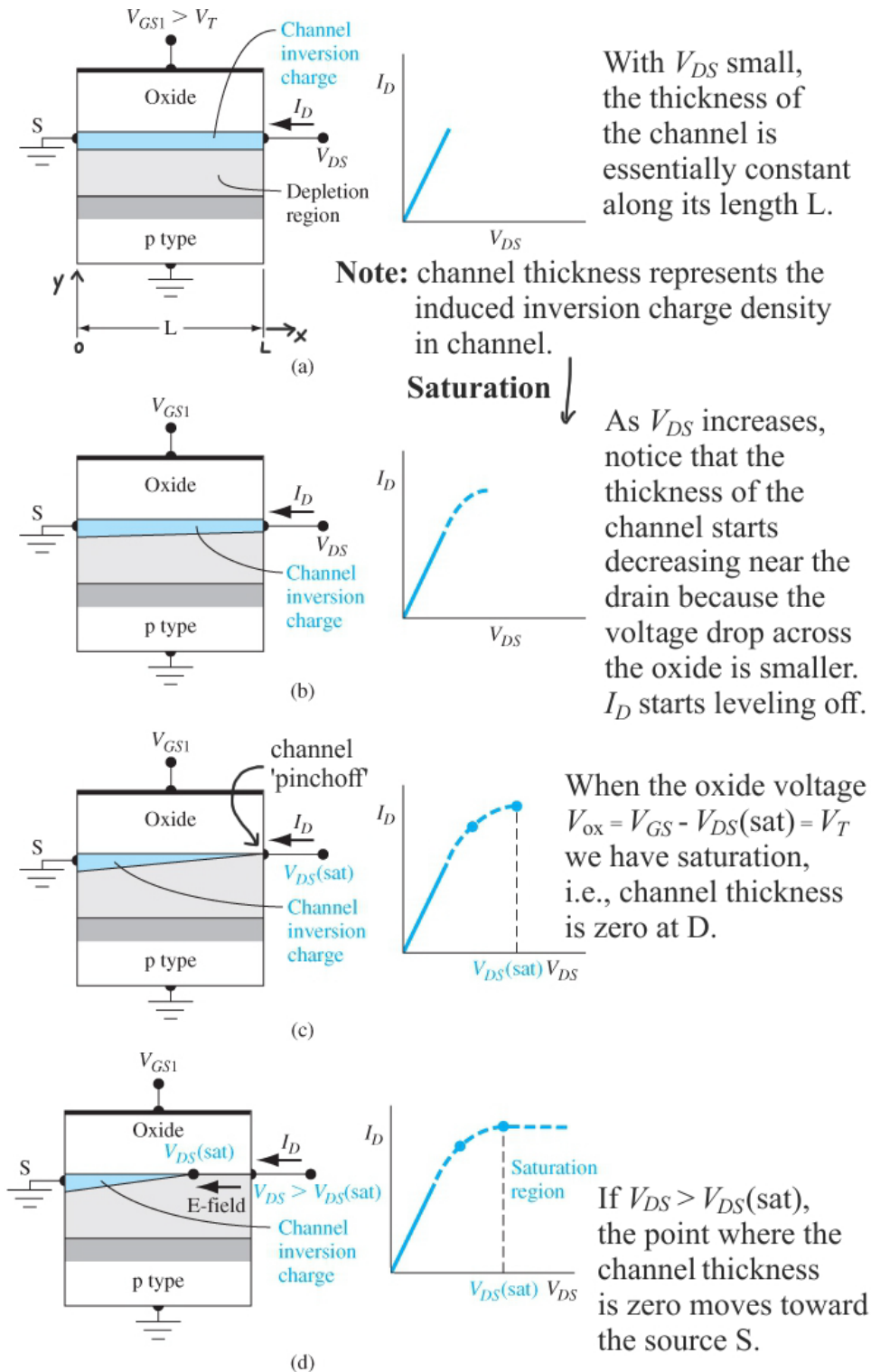


Figure 10.39 | Cross section and I_D versus V_{DS} curve when $V_{GS} < V_T$ for (a) a small V_{DS} value, (b) a larger V_{DS} value, (c) a value of $V_{DS} = V_{DS(sat)}$, and (d) a value of $V_{DS} > V_{DS(sat)}$.

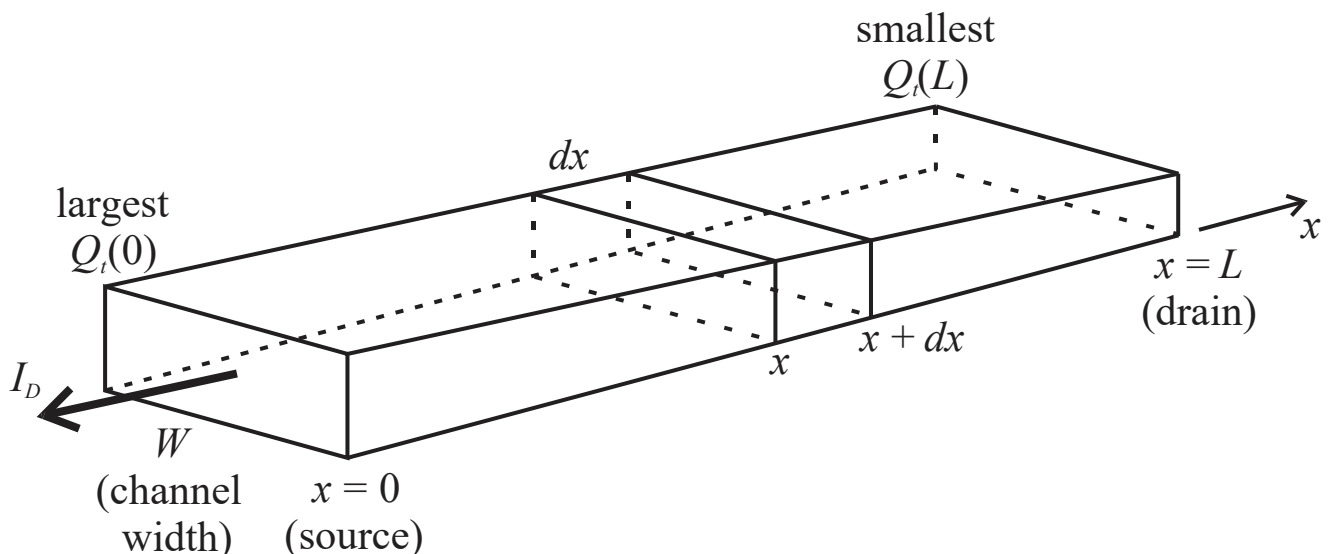
➤ Saturation voltage **$V_{DS(sat)} = V_{GS} - V_T$** . Saturation is a reason to set V_{GS} greater than the minimum required to achieve threshold, i.e., set $V_{GS} > V_T$.

10.3.3 Current-Voltage Relationship- Derivation

We want to find I_D as a function of V_{DS} (and V_{GS}). We'll take a different approach than the text.

Key Assumptions

- 1) Current in the channel is drift current NOT diffusion.
 - 2) No current flows through oxide, i.e., $I_G = 0$.
 - 3) Current flows in the x -direction (side-to-side) w/ little/no current flow up-n-down or in-n-out, AKA 'gradual channel' approximation.
 - 4) Charge in the oxide represented by a fixed surface charge density at the oxide-substrate boundary/interface.
 - 5) Carrier mobility μ in the channel is constant.
- As we saw in Fig. 10.39, the channel 'tilts' along its length L (x -direction) as V_{DS} increases. To characterize this, define a channel voltage $V_C(x)$ along the channel ($0 \leq x \leq L$) where $V_C(x=0) = V_S = 0$ (grounded) and $V_C(x=L) = V_{DS}$ (at drain).
- Assume the entire channel is inverted. This implies $V_{DS} \geq V_T$ and that the voltage between the gate and drain $V_{GD} = V_{GS} - V_{DS} \geq V_T$.
- Also, define the total mobile charge density $Q_i(x)$ for $0 \leq x \leq L$ in the channel, it will be proportional to the height/thickness of the channel.



- In terms of capacitance $Q_t(x) = -C_{ox}[(V_{GS} - V_T) - V_C(x)]$ for $0 \leq x \leq L$. [Note: The difference $V_{GS} - V_T$ is how much the gate voltage is above the threshold voltage, i.e., available to form the channel.]
- We can get the incremental resistance of the channel over length dx , by adapting $R = \frac{\ell}{\sigma A}$, to get $dR = \frac{-dx}{W Q_t(x) \mu_n}$. [Note: Per Chapter 5, $\sigma_n = e\mu_n n$.]
- By Ohm's Law, $dV_C = I_D dR = \frac{-I_D dx}{W Q_t(x) \mu_n}$.
- Re-arrange and integrate to get

$$\begin{aligned} \int_{x=0}^L I_D dx &= -W \mu_n \int_{V_C=0}^{V_{DS}} Q_t(x) dV_C \\ &= W \mu_n C_{ox} \int_{V_C=0}^{V_{DS}} [(V_{GS} - V_T) - V_C(x)] dV_C \\ I_D L &= W \mu_n C_{ox} \left[(V_{GS} - V_T)V_C - \frac{V_C^2}{2} \right]_{V_C=0}^{V_{DS}} \\ I_D &= \frac{W}{L} \mu_n C_{ox} \left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right] \end{aligned}$$

$$\boxed{I_D = \frac{W \mu_n C_{ox}}{2L} \left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2 \right]} \quad (10.62)$$

where $0 \leq V_{DS} \leq V_{DS}(\text{sat})$ (below saturation) and $V_{GS} \geq V_T$ (inverted) for the **Linear Region** of the MOSFET. This can also be written as

$$\boxed{I_D = \frac{k_n'}{2} \frac{W}{L} \left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2 \right] = K_n \left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2 \right]} \quad (10.63)$$

where k_n' (A/V^2) is the process conduction parameter and K_n (A/V^2) is the conduction parameter.

What about when we hit saturation, i.e., $V_{DS} \geq V_{DS}(\text{sat}) = V_{GS} - V_T$ (10.64) and $V_{GS} \geq V_T$ (inverted), where I_D starts leveling off?

Using $V_{DS}(\text{sat})$ in (10.62), we get

$$I_D(\text{sat}) = \frac{W \mu_n C_{\text{ox}}}{2L} \left[2(V_{GS} - V_T)V_{DS}(\text{sat}) - V_{DS}^2(\text{sat}) \right] \quad (10.63)$$

This **constant** saturation current value can also be written as

$$I_D(\text{sat}) = \frac{W \mu_n C_{\text{ox}}}{2L} (V_{GS} - V_T)^2 \quad (10.66)$$

$$\text{or } I_D(\text{sat}) = \frac{k'_n W}{2 L} (V_{GS} - V_T)^2 = K_n (V_{GS} - V_T)^2 \quad (10.67).$$

Remember, if $V_{GS} < V_T \Rightarrow$ no inversion layer \Rightarrow **Cutoff Mode/Region** of the MOSFET with $I_D \approx 0$.

Figures 10.40 and 10.42 show some I - V curves for n-channel (p-type substrate) MOSFETs.

From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.

n-channel enhancement mode MOSFET

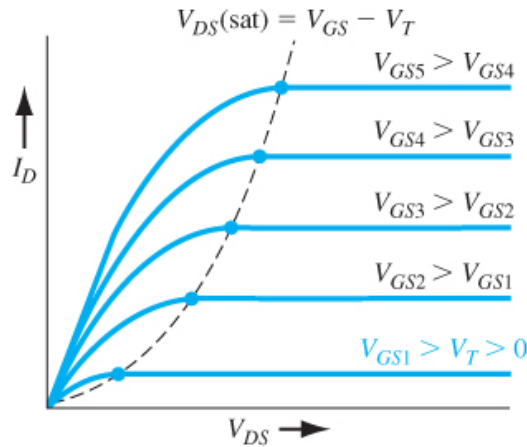


Figure 10.40 | Family of I_D versus V_{DS} curves for an n-channel enhancement mode MOSFET.

- Here, the gate voltage must be positive and greater than the threshold voltage to create a channel, i.e., $V_{GS} > V_T > 0$.
- Note how both the drain saturation voltage $V_{DS}(sat)$ and saturation current $I_D(sat)$ increase as the gate voltage V_{GS} increases.

n-channel depletion mode MOSFET

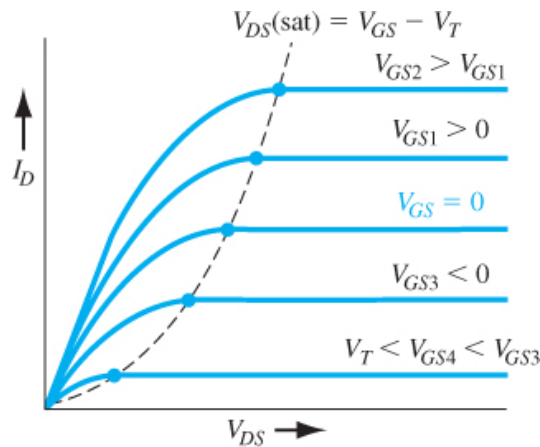
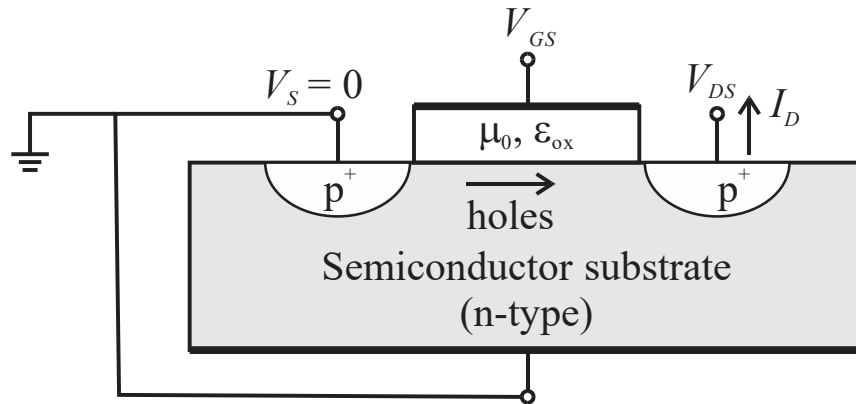


Figure 10.42 | Family of I_D versus V_{DS} curves for an n-channel depletion mode MOSFET.

- Here, an inversion layer or channel exists with no voltage applied to the gate.
- So, we can have $I-V$ curves with $V_{GS} < 0$.

What about **p-channel MOSFETs** with n-type substrates?



Note: Typically, $V_{GS} < 0$ and $V_{DS} < 0$.

Here, $V_{DS}(\text{sat}) = V_{GS} - V_T$

Linear Region [$V_{GS} \leq V_T$ (inverted) & $V_{DS}(\text{sat}) \leq V_{DS} \leq 0$ (not saturated)
or $|V_{DS}| < |V_{GS} - V_T|$]

$$I_D = \frac{W \mu_p C_{\text{ox}}}{2L} [2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$$

where and for the of the MOSFET. This can also be written as

$$I_D = \frac{k'_n W}{2L} [2(V_{GS} - V_T)V_{DS} - V_{DS}^2] = K_n [2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$$

where k'_n is the process conduction parameter and K_n is the conduction parameter.

Saturation [$V_{GS} \leq V_T$ (inverted) & $V_{DS} \leq V_{DS}(\text{sat})$ (saturated)]

$$I_D(\text{sat}) = \frac{W \mu_p C_{\text{ox}}}{2L} (V_{GS} - V_T)^2$$

This **constant** saturation current value can also be written as

$$I_D(\text{sat}) = \frac{k'_n W}{2L} (V_{GS} - V_T)^2 = K_n (V_{GS} - V_T)^2$$

Remember, if $V_{GS} > V_T \Rightarrow$ no inversion layer \Rightarrow **Cutoff Mode/Region** of the MOSFET with $I_D \approx 0$.

➤ The text uses an alternative layout w/ $V_{SG} = -V_{GS}$ and $V_{SD} = -V_{DS}$.

From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.

p-channel MOSFET

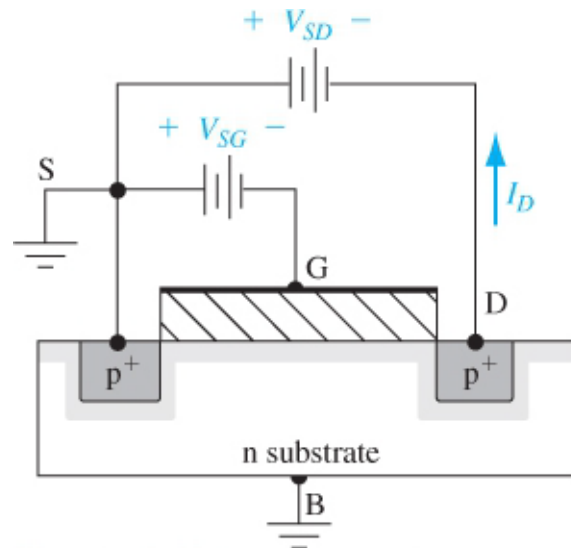


Figure 10.49 | Cross section and bias configuration for a p-channel enhancement mode MOSFET.

➤ Here, $V_{SG} = -V_{GS} > 0$ and $V_{SD} = -V_{DS} > 0$. Positive charges (holes) flow through p-channel from source (S) to drain (D) and I_D **emerges** from drain.

➤ **Linear region**
$$I_D = \frac{W \mu_p C_{ox}}{2L} [2(V_{SG} + V_T)V_{SD} - V_{SD}^2] \quad (10.70)$$

where $0 \leq V_{SD} \leq V_{SD}(\text{sat})$ [or $V_{SD} < V_{SG} + V_T$] **and** $V_{SG} \geq V_T$.

➤ **Saturation region**
$$I_D(\text{sat}) = \frac{W \mu_p C_{ox}}{2L} (V_{SG} + V_T)^2 \quad (10.72)$$

where $V_{SD} \geq V_{SD}(\text{sat})$ **and** $V_{SG} \geq V_T$.

➤ Saturation voltage
$$V_{SD}(\text{sat}) = V_{SG} + V_T \quad (10.74)$$

➤ Threshold voltage $V_T < 0$ for an **enhancement mode** p-channel MOSFET.

➤ Threshold voltage $V_T > 0$ for a **depletion mode** p-channel MOSFET where the inversion layer exists when $V_{GS} = V_{SG} = 0$.

➤ If $V_{SG} < V_T \Rightarrow$ no inversion layer \Rightarrow **Cutoff Mode/Region** w/ $I_D \approx 0$.

10.3.4 Transconductance

For an n-channel (p-type substrate) MOSFET, the transconductance, i.e., the transistor gain, is

$$\boxed{g_m = \frac{\partial I_D}{\partial V_{GS}}} \quad (10.75).$$

Why V_{GS} ? Typically, the small AC voltage signal that we want to amplify is applied (on top of the DC V_{GS}) to the gate terminal of the MOSFET to cause amplified AC variations in the drain current I_D , i.e., a MOSFET amplifier is a VCCS (voltage-controlled current source)

Linear mode/region,

$$g_m = \frac{\partial}{\partial V_{GS}} \left(\frac{W \mu_n C_{ox}}{2L} \left[2(V_{GS} - V_T) V_{DS} - V_{DS}^2 \right] \right)$$

$$\boxed{g_{mL} = g_m = \frac{W \mu_n C_{ox}}{L} V_{DS}} \quad (10.76).$$

Saturation mode/region,

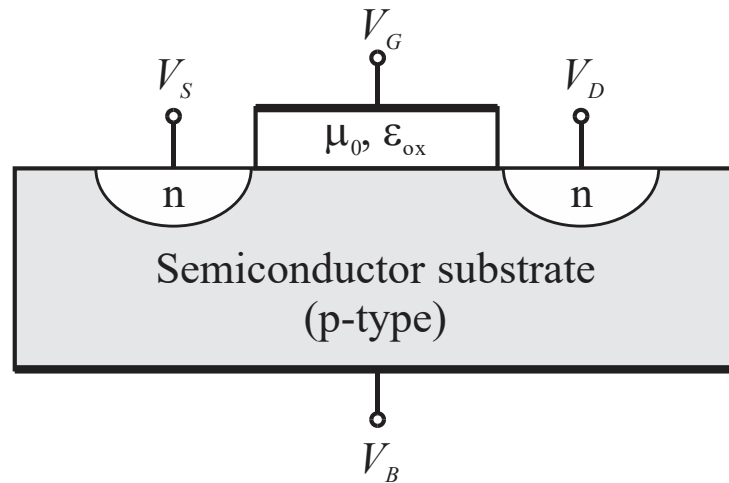
$$g_m = \frac{\partial}{\partial V_{GS}} \left(\frac{W \mu_n C_{ox}}{2L} (V_{GS} - V_T)^2 \right)$$

$$\boxed{g_{mS} = g_m = \frac{W \mu_n C_{ox}}{L} (V_{GS} - V_T)} \quad (10.77).$$

- The transconductance depends on MOSFET geometry/materials- W/L ratio, μ_n , and C_{ox} .
- In linear mode, transconductance depends on V_{DS} .
- In saturation mode, transconductance depends on V_{GS} .

10.3.5 Substrate Bias Effects

Up to now, we have let $V_S = V_B = 0$ (both grounded) for an n-channel (p-type substrate).



What if $V_B > V_S$?

- This creates a **forward-biased** pn junction between the substrate and the source \Rightarrow LARGE amount of current flows across this junction, i.e., MOSFET melts! [This is considered *bad*.]

Therefore, we could try $V_B < V_S$ or $V_{SB} = V_S - V_B \geq 0$, i.e., keep this pn junction **reverse-biased**. If $V_{SB} > 0$, the thickness of the depletion layer at this junction will increase \Rightarrow shifts the threshold voltage V_T .

w/ $V_{SB} = 0$

$$Q'_{SD}(\text{max}) = -e N_a x_{dT} = -\sqrt{2e\epsilon_s N_a (2\phi_{fp})} \quad (10.78).$$

w/ $V_{SB} > 0$

$$Q'_{SD} = -e N_a x_d = -\sqrt{2e\epsilon_s N_a (2\phi_{fp} + V_{SB})} \quad (10.79)$$

with a corresponding change in space charge density of

$$\Delta Q'_{SD} = -\sqrt{2e\epsilon_s N_a} \left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}} \right] \quad (10.80).$$

This implies that the threshold voltage change is

$$\Delta V_T = \frac{-\Delta Q'_{SD}}{C_{ox}} = \frac{\sqrt{2e\epsilon_s N_a}}{C_{ox}} \left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}} \right] \quad (10.81)$$

where $\Delta V_T = V_T(V_{SB} > 0) - V_T(V_{SB} = 0) = V_T(V_{SB} > 0) - V_{T0} > 0$.

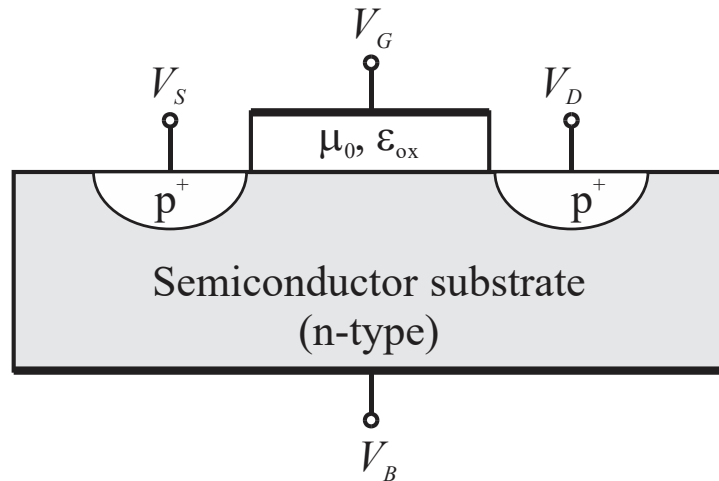
ΔV_T can be put in terms of a body-effect coefficient

$$\gamma = \frac{\sqrt{2e\epsilon_s N_a}}{C_{ox}} \quad (V^{0.5}) \quad (10.82)$$

as $\Delta V_T = \gamma \left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}} \right] \quad (10.83)$.

Also, $V_T = V_{T0} + \Delta V_T = V_{T0} + \gamma \left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}} \right]$ (Note: $V_{T0} = V_{TN}$.)

p-channel (n-type substrate)



Here, we change polarities on several voltages to get-

$$\gamma = \frac{\sqrt{2e\epsilon_s N_d}}{C_{ox}} \quad (V^{0.5}) \quad \text{and} \quad \Delta V_T = -\gamma \left[\sqrt{2\phi_{fn} + V_{BS}} - \sqrt{2\phi_{fn}} \right]$$

Example- Let's revisit our earlier example where we found the flat band voltage and threshold voltage for a MOS capacitor at 300 K with a gold metal gate. Now, let's assume it is used to make an n-channel MOSFET where we apply $V_{SB} = 1$ V and see how things change. It has a silicon dioxide for the oxide layer of thickness 21 nm with an equivalent trapped charge density of 2×10^{11} cm⁻² and a p-type silicon substrate where $N_a = 10^{17}$ cm⁻³.

From prior example (assumed $V_{SB} = 0$ V)-

From Table B.4, $n_i = 1.5 \times 10^{10}$ cm⁻³, $\epsilon_{s, Si} = 11.7 \epsilon_0$, and $\epsilon_{s, SiO_2} = 3.9 \epsilon_0$ at 300 K.

$$C_{ox} = \epsilon_{ox} / t_{ox} \Rightarrow \underline{C_{ox} = 1.64435 \times 10^{-3} \text{ F/m}^2 = 1.64435 \times 10^{-7} \text{ F/cm}^2}.$$

Equivalent trapped charge density is $\Rightarrow \underline{Q'_{ss} = 3.204353 \times 10^{-8} \text{ C/cm}^2}$.

From Fig. 10.16, the metal-semiconductor work function is $\Rightarrow \underline{\phi_{ms} = -0.13 \text{ V}}$.

Per (10.25), the flat-band voltage is $\Rightarrow \underline{V_{FB} = -0.32487 \text{ V}}$.

$$\text{Per (10.4), } \phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = 0.025852 \ln\left(\frac{10^{17}}{1.5 \cdot 10^{10}}\right) \Rightarrow \underline{\phi_{fp} = 0.406203 \text{ V}}.$$

Per (10.6), the maximum depletion layer width is $\Rightarrow \underline{x_{dT} = 1.024976 \times 10^{-7} \text{ m}}$.

Per (10.27), $\Rightarrow \underline{|Q_{SD}'(\text{max})| = 1.64435 \times 10^{-3} \text{ C/m}^2 = 1.64435 \times 10^{-7} \text{ C/cm}^2}$.

Per (10.31c), the threshold voltage is $\Rightarrow \underline{V_{TN} = 1.48622 \text{ V}}$.

$$\boxed{V_{SB} = 1 \text{ V}}$$

Using (10.79), calculate the space charge density to now be

$$\begin{aligned} Q'_{SD} &= -eN_a x_d = -\sqrt{2e\epsilon_s N_a (2\phi_{fp} + V_{SB})} \\ &= -\sqrt{2(1.6022 \cdot 10^{-19}) 11.7 (8.8542 \cdot 10^{-12}) 10^{23} (2(0.406203) + 1)} \\ &\Rightarrow \underline{Q'_{SD} = -2.45282 \times 10^{-3} \text{ C/m}^2 = -2.45282 \times 10^{-7} \text{ C/cm}^2}. \end{aligned}$$

Using (10.80), the change in the space-charge density is

$$\begin{aligned}\Delta Q'_{SD} &= -\sqrt{2e\epsilon_s N_a} \left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}} \right] \\ &= -\sqrt{2(1.6022 \cdot 10^{-19})11.7(8.8542 \cdot 10^{-12})10^{23}} \left[\sqrt{2(0.4062) + 1} - \sqrt{2(0.4062)} \right] \\ &\Rightarrow \underline{\Delta Q'_{SD} = -8.10625 \times 10^{-4} \text{ C/m}^2 = -8.10625 \times 10^{-8} \text{ C/cm}^2}.\end{aligned}$$

Calculate the body-effect coefficient using (10.82),

$$\begin{aligned}\gamma &= \frac{\sqrt{2e\epsilon_s N_a}}{C_{ox}} = \frac{\sqrt{2(1.6022 \cdot 10^{-19})11.7(8.8542 \cdot 10^{-12})10^{23}}}{1.64435 \cdot 10^{-3}} \\ &\Rightarrow \underline{\gamma = 1.108009 \text{ V}^{0.5}}.\end{aligned}$$

Calculate the change in threshold voltage using (10.83),

$$\begin{aligned}\Delta V_T &= \gamma \left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}} \right] = 1.108009 \left[\sqrt{2(0.4062) + 1} - \sqrt{2(0.4062)} \right] \\ &\Rightarrow \underline{\Delta V_T = 0.492976 \text{ V}}.\end{aligned}$$

Calculate the new threshold voltage-

$$V_T = V_{T0} + \Delta V_T = V_{TN} + \Delta V_T = 1.48622 + 0.492976 \Rightarrow \underline{V_T = 1.9792 \text{ V}}.$$

10.4 Frequency Limitations

- MOSFETs used in linear amplifiers are typically represented by a small-signal equivalent circuit model w/ a VCCS (voltage-controlled current source).
- Parts of this model will explain the MOSFET frequency limitations.

10.4.1 Small-Signal Equivalent Circuit

From *Semiconductor Physics and Devices: Basic Principles* (4th Edition), Donald A. Neamen, McGraw Hill, 2012, ISBN 978-0-07-352958-5.

n-channel MOSFET

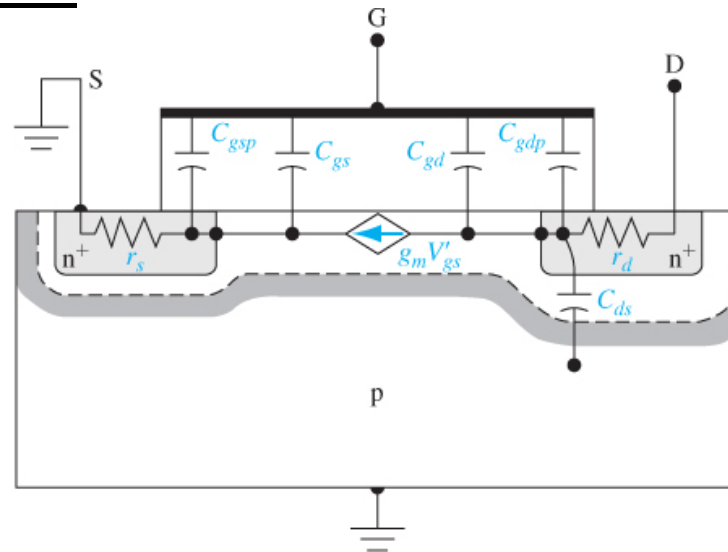


Figure 10.52 | Inherent resistances and capacitances in the n-channel MOSFET structure.

- Note that the body (B) and source (S) are both grounded (common-source).
- There are gate-source C_{gs} and gate-drain C_{gd} capacitances to represent the interaction between the gate and the channel charges on each end (D & S).
- In addition, there are **parasitic** gate-source C_{gsp} and gate-drain C_{gdp} capacitances due to manufacturing issues which cause gate oxide and the drain & source regions to overlap. $C_{gsp} = C_{ox}$ (gate-source overlap area) and $C_{gdp} = C_{ox}$ (gate-drain overlap area).
- There is a drain-to-substrate C_{ds} capacitance to represent the pn junction capacitance. [Not needed for source-to-substrate as they are both grounded.]
- The drain and source will have some series resistances, r_d and r_s .
- Lastly, we have the voltage-controlled current-source (VCCS) element, $g_m V_{gs}'$, to represent the I - V relation of the MOSFET.
- The transconductance g_m was defined earlier.
- The internal gate-to-source voltage is V_{gs}' is what controls the current through the channel. It is the gate-to-source voltage less the voltage drop across the source resistance r_s .

Small-signal circuit model for common-source n-channel MOSFET

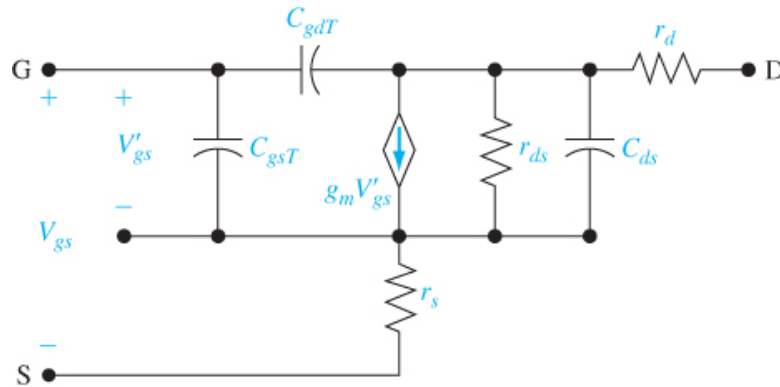


Figure 10.53 | Small-signal equivalent circuit of a common-source n-channel MOSFET.

- This small-signal model uses total gate-source $C_{gsT} = C_{gs} + C_{gsp}$ and total gate-drain $C_{gdT} = C_{gd} + C_{gdp}$ capacitances, i.e., combine regular and parasitic capacitances.
- Model adds a resistance r_{ds} to account for slope of MOSFET $I-V$ curve. In saturation, $r_{ds} \rightarrow \infty$.
- For p-channel model, reverse voltage polarities and current directions.

Low frequency small-signal circuit models

- At low frequencies, the capacitors act like open circuits.
- Note that the impedance looking into the gate is infinite in both models.

Model 1

- Neglect r_s and r_d , but keep r_{ds} .

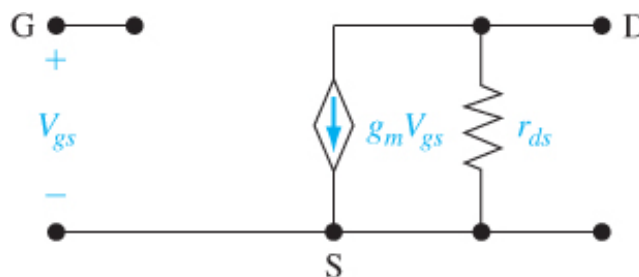


Figure 10.54 | Simplified, low-frequency small-signal equivalent circuit of a common-source n-channel MOSFET.

Model 2

- Neglect r_{ds} and r_d , but keep r_s .

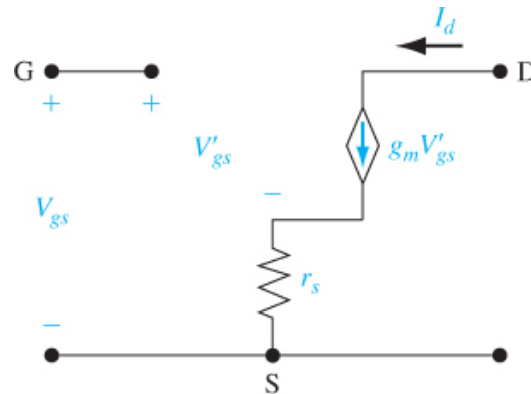


Figure 10.55 | Simplified, low-frequency small-signal equivalent circuit of common-source n-channel MOSFET including source resistance r_s .

- Here, $I_d = g_m V'_{gs}$ (10.84).
- By KVL, $V_{gs} = V'_{gs} + I_d r_s = V'_{gs} + g_m V'_{gs} r_s = (1 + g_m r_s) V'_{gs}$.
- Combining these two equations, we get $I_d = \left(\frac{g_m}{1 + g_m r_s} \right) V_{gs} = g'_m V_{gs}$ (10.86)

where $g'_m = \frac{g_m}{1 + g_m r_s}$ is the effective transconductance which is less than g_m .

10.4.2 Frequency Limitation Factors and Cut-off Frequency

What limits the upper frequency for MOSFETs in amplifiers?

Channel transit time (usually not the critical limiting effect)

- Charge carriers move at some velocity v_{sat} (m/s). This implies that the charges take some transit time τ_t to cross the channel, i.e., $\tau_t = L / v_{\text{sat}}$ (s).
- We can define an upper frequency limit to account for this as $f_{\text{limit}} = 1/\tau_t$.

Example- If $L = 1 \mu\text{m}$ and $v_{\text{sat}} = 5 \times 10^6 \text{ cm/s} = 5 \times 10^4 \text{ m/s}$, find τ_t & f_{limit} .

$$\tau_t = 10^{-6} / 5 \times 10^4 \quad \Rightarrow \quad \underline{\tau_t = 2 \times 10^{-11} \text{ s} = 20 \text{ ps.}}$$

$$f_{\text{limit}} = 1/2 \times 10^{-11} \quad \Rightarrow \quad \underline{f_{\text{limit}} = 5 \times 10^{10} \text{ Hz} = 50 \text{ GHz.}}$$

Capacitance (AKA gate/capacitance charging time)

- Define a cutoff frequency in terms of an equivalent gate capacitance

$$f_T = \frac{g_m}{2\pi(C_{gsT} + C_M)} = \frac{g_m}{2\pi C_G} \quad (10.95).$$

- The equivalent gate capacitance $C_G = C_{gsT} + C_M$.

- The term C_M is the *Miller capacitance* defined as

$$C_M = C_{gdT}(1 + g_m R_L) \quad (10.91)$$

where R_L is the load resistance connected to the drain, $C_{gdT} = C_{gd} + C_{gdp}$, and $C_{gsT} = C_{gs} + C_{gsp}$.

- In saturation, $C_{gs} \rightarrow C_{\text{ox}} WL$ and $C_{gd} \rightarrow 0$. The parasitic capacitances, i.e., C_{gdp} and C_{gsp} , are not affected by saturation or lack thereof. This means $C_M \neq 0$ because $C_{gsT} \rightarrow C_{\text{ox}} WL + C_{gsp}$ and $C_{gdT} \rightarrow C_{gdp}$.

- An **ideal** MOSFET has no overlap, i.e., $C_{gsp} = C_{gdp} = 0$. Therefore, in saturation, $C_{gsT} = C_{gs} = C_{\text{ox}} WL$ and $C_{gdT} = 0$. Using g_{mS} from (10.77), we get

$$f_T = \frac{g_{mS}}{2\pi C_G} = \frac{\mu_n (V_G - V_T)}{2\pi L^2} \quad (10.96).$$

Example- An n-channel silicon MOSFET has a channel length of 0.72 μm , width of 3.1 μm , an electron mobility of 1000 $\text{cm}^2/\text{V}\cdot\text{s}$, saturation velocity of 8×10^6 cm/s , and a threshold voltage of 1.4 V at 300 K. The gate oxide overlaps the drain and source contacts by 60 nm. It has an oxide (SiO_2) layer thickness of 16 nm. If the MOSFET is in saturation with $V_{GS} = 5$ V and has a 6 k Ω load, find the transit time cutoff frequency, cutoff frequency, and ideal cutoff frequency.

From Table B.4 and Table B.6, silicon has $n_i = 1.5 \times 10^{10}$ cm^{-3} , $\epsilon_{s,\text{Si}} = 11.7\epsilon_0$, and $\epsilon_{s,\text{SiO}_2} = 3.9\epsilon_0$ at 300 K.

From section 10.4.2 of the text, the channel transit time is

$$\tau_t = L/v_{\text{sat}} = 0.72 \times 10^{-6} \text{ m} / 8 \times 10^4 \text{ m/s} \Rightarrow \underline{\tau_t = 9 \times 10^{-12} \text{ s} = 9 \text{ ps.}}$$

This leads to transit time cutoff frequency of

$$f_{\text{limit}} \cong 1/\tau_t = 1/9 \times 10^{-12} \Rightarrow \underline{f_{\text{limit}} = 111.1 \text{ GHz (not an issue).}}$$

Using (10.35), the oxide capacitance per unit area is

$$C_{ox} = \epsilon_{ox}/t_{ox} = 3.9(8.8541878 \times 10^{-12} \text{ F/m})/16 \times 10^{-9} \text{ m} \\ \Rightarrow \underline{C_{ox} = 2.15821 \times 10^{-3} \text{ F/m}^2 = 2.15821 \times 10^{-7} \text{ F/cm}^2.}$$

The gate-drain & gate-source overlap areas are

$$A_{\text{overlap}} = \text{overlap}(W) = 60 \times 10^{-9} (3.1 \times 10^{-6}) \Rightarrow \underline{A_{\text{overlap}} = 1.86 \times 10^{-13} \text{ m}^2.}$$

The gate-drain & gate-source parasitic capacitances are-

$$C_{gdp} = C_{gsp} = C_{ox} (A_{\text{overlap}}) = 2.15821 \times 10^{-3} (1.86 \times 10^{-13}) \\ \Rightarrow \underline{C_{gdp} = C_{gsp} = 4.01427 \times 10^{-16} \text{ F.}}$$

Per p. 427 of text, with the MOSFET in saturation, $\underline{C_{gd} \rightarrow 0}$ and

$$C_{gs} = C_{ox} WL = 2.15821 \times 10^{-3} (3.1 \times 10^{-6}) 0.72 \times 10^{-6} \Rightarrow \underline{C_{gs} = 4.81712 \times 10^{-15} \text{ F.}}$$

Now, the total gate-drain & gate-source capacitances are-

$$C_{gdT} = C_{gd} + C_{gdp} = 0 + 4.01427 \times 10^{-16} \Rightarrow \underline{C_{gdT} = 4.01427 \times 10^{-16} \text{ F}}, \text{ and}$$

$$C_{gsT} = C_{gs} + C_{gsp} = 4.81712 \times 10^{-15} + 4.01427 \times 10^{-16} \Rightarrow \underline{C_{gsT} = 5.21855 \times 10^{-15} \text{ F}}.$$

To find the Miller capacitance C_M , we will need the transconductance g_m of the MOSFET. In saturation, the transconductance is (10.77)

$$g_{ms} = \frac{W \mu_n C_{ox}}{L} (V_{GS} - V_T) = \frac{3.1 \cdot 10^{-6} (1000) 2.15821 \cdot 10^{-7}}{0.72 \cdot 10^{-6}} (5 - 1.4)$$

$$\Rightarrow \underline{g_{ms} = 3.345223 \times 10^{-3} \text{ S}}.$$

Per (10.91), the Miller capacitance is

$$C_M = C_{gdT} (1 + g_{ms} R_L) = 4.01427 \times 10^{-16} [1 + (3.345223 \times 10^{-3}) 6 \times 10^3]$$

$$\Rightarrow \underline{C_M = 8.4586 \times 10^{-15} \text{ F}}.$$

Per (10.95), the cutoff frequency is-

$$f_T = \frac{g_{ms}}{2\pi(C_{gsT} + C_M)} = \frac{3.345223 \cdot 10^{-3}}{2\pi(5.21855 \cdot 10^{-15} + 8.4586 \cdot 10^{-15})}$$

$$\Rightarrow \underline{f_T = 3.89269 \times 10^{10} \text{ Hz} = 38.93 \text{ GHz}}.$$

Per (10.96), the ideal cutoff frequency is-

$$f_{T,\text{ideal}} = \frac{\mu_n (V_{GS} - V_T)}{2\pi L^2} = \frac{1000 (10^{-4}) (5 - 1.4)}{2\pi (0.72 \cdot 10^{-6})^2}$$

$$\Rightarrow \underline{f_{T,\text{ideal}} = 1.10524 \times 10^{11} \text{ Hz} = 110.52 \text{ GHz}}.$$

The parasitic capacitances make a difference!