CENG 244/L Introduction to Digital Systems (3-1), SDSM&T, Spring 2014

Lecture Room & Time: EP254 MWF from 3-3:50 pm

Laboratory Room & Times: EP336/342 Tu from noon-1:50 pm (-51) & 2-3:50 pm (-52)

Instructor: Dr. Thomas Montoya, EP325, Tel: 394-2459, e-mail: Thomas.Montoya@sdsmt.edu

Office Hours: noon-1 pm MWF, or when available.

WWW: See link from http://montoya.sdsmt.edu. The course web page will be heavily utilized for posting **assignments**, examples, solutions, ... E-mail will be utilized to notify students of course-related information and events (**check daily**). Your first.last@Mines.sdsmt.edu address will be used.

Catalog Description: This course is designed to provide computer engineering, electrical engineering, and computer science students with an understanding of the basic concepts of digital systems and their hardware implementation. Topics covered include combinational logic circuits, sequential logic circuits, and CPU control.

CENG 244 Prerequisite: MATH 102 (College Algebra) or equivalent.

CENG 244 Corequisite: CENG 244L

Text: *Digital Design*, Fifth Edition, M. Morris Mano and Michael D. Ciletti, Prentice Hall, 2013, ISBN-10: 0-13-277420-8 • ISBN-13: 978-0-13-277420-8.

Course Policies:

- Course instruction will be delivered in lectures. Attendance is required. Notify instructor in advance (when possible) if you will be absent from class.
- **Laboratory**- You must register for one of the CENG 244L sections. Laboratory assignments and completion dates will be announced and distributed as they occur. Further laboratory information and policies will be given during the initial laboratory meeting.
- Except when otherwise specified, all coursework is to be individually completed. Also, see the *Conduct* section in the catalog and the *Student Conduct* web page for SDSM&T (see information at http://www.sdsmt.edu/Campus-Life/Student-Resources/Student-Conduct/).
- Students are encouraged to discuss homework/laboratories with classmates in general terms. However, copying, plagiarism … is not acceptable and will be penalized.
- Homework (HW) is due at the beginning of class on the specified days (up to 20% penalty for being late w/out doctor's note …). If you know that you will be missing a class, it may be turned in early. HW will **not** be graded after solutions are posted on the course web page.
- Bring notes and text to **every** class. Most quizzes will be unannounced and require a calculator. Occasionally a quiz may be open book/notes (no borrowing).
- Missed quizzes will **not** be made up. If you know that you will be missing a class for a school-related activity (athletic travel, academic conference, etc.), you may stop by the day before and ask to take a quiz early (if available).
- If 2/3 of quizzes **and** 2/3 of HW are completed at a **passing** level, the lowest HW grade and lowest two quiz grades will be dropped (no questions asked). If not, **all** quizzes and HW will count (no drops). The drops are meant to cover all absences, including those due to illness, interviews, trips…
- **All** laboratories must be completed by **every individual** at a passing level to pass the class.

- To facilitate grading, homework shall meet the following specifications (see HW example on course web page):
  (a) Use the **front side only** (i.e., single-sided) of 8.5" × 11" engineering graph paper or plain white paper (NO pages torn from spiral notebooks) for assignments.
  (b) At the top of **every** page put the date, course number, HW #, problem number(s) as **per text** (if applicable), your name, and the page numbering (i.e., page *x* of *y* or *x*/*y* formats in the upper right hand corner). Ensure problems & pages are in order.
  (c) All work exceeding one page should be stapled - no paper clips, folded corners, or folders.
  (d) Copy, paraphrase, or cut-n-paste problem descriptions, figures, and/or circuits and **show all** work so it can be understood without the text. No work/"magic" answer → no credit.
  (e) Reference equations derived in the text (e.g., equation number and/or page number). Fundamental equations (e.g., Maxwell's equations, Ohm's Law ...) are excluded from this requirement.
  (f) Writing/figures/graphs must be legible & large enough to read → illegible = no credit.
  (g) Answers should be boxed/double underlined, in **decimal** format (if numbers), and the variables, values & units (if any) included. Use lead zeros for fractional answers, e.g., 0.4 not ".4".
  (h) Where applicable, use conventional engineering units such as millivolts (mV), picoseconds (ps), gigahertz (GHz) … Answers without applicable units are incomplete/incorrect.
  (i) Work problems sequentially in a **single** vertical column with subparts clearly labeled, e.g., a), b) ... Leave space (e.g., 1/2") between consecutive parts of a problem, and draw a line across the page at the end of each problem if there is more than one. **No more than two problems on any page.**

Course Goals: The objective of this course is to provide students with an understanding of the basic concepts associated with the analysis and design of combinational and sequential circuits. Combinational circuits include AND, OR, NOT, NAND, and NOR logic gates, adders, code converters, and memory devices. Sequential circuits include flip-flops, registers, counters, and programmable logic devices.

Student Learning Outcomes:

Upon completion of this course, students should demonstrate the ability to:

1. Convert numbers between binary and decimal, binary and hexadecimal, and decimal and binary coded decimal notation.
2. Perform the mathematical operations of addition, subtraction, multiplication, and division using signed and unsigned binary numbers.
3. Analyze combinational logic circuits using AND, NOT, OR, NOR, NAND, and XOR logic gates.
4. Design combinational logic circuits using truth tables and Karnaugh maps.
5. Program EPROMs and PALs.
6. Analyze sequential logic circuits and prepare timing diagrams using Flip-Flop Characteristic Tables.
7. Design sequential logic circuits using state diagrams, state tables, and Flip-Flop Excitation Tables.
8. Construct logic circuits in the laboratory using student trainer boards.
9. Design and construct digital control and data processing circuits using ASM charts to define digital hardware algorithms.

Electronic Devices Policy: Unless otherwise specified, no electronic devices are to be used during class. I.e., turn off your cell phone before class starts, **no** text messaging, & **no** headphones. An exception is that you may use a tablet for purposes of note taking.

ADA: Students with special needs or requiring special accommodations should contact the instructor and/or the campus ADA coordinator, Jolie McCoy, at 394-1924 at the earliest opportunity.

Evaluation:		
	3 Hour Exams @ 10%/each	30%
	Quizzes*	15%
	Homework*	10%
	Laboratory (e.g., logbook, report(s), etc)*	25%
	Final Exam (required)	20%
	**Total	**100%**

* see course policies

Grading scale: 100 > A > 90, 89 > B > 80, 79 > C > 70, 69 > D > 60, F < 60.

Intergrity Policy: Note that according to "Cheating (Academic Integrity) Policy" in the SDSM&T Undergraduate Catalog, "The consequences for any act of academic dishonesty shall be at the discretion of the instructor of record, subject to due process as outlined in BOR policy 3.4.3A. Sanctions may range from requiring the student to repeat the work in question to failure in the course."

Exams/Quizzes:

- No electronic device can be present during an exam. All cell phones, audio players, calculators (unless specified by instructor), PDA, computer, etc must be turned off and put away during exams.
- No beverage containers are allowed in the exam.
- All hats must be removed and put away.
- Instructor may assign random seating at exams.
- Different versions of exam(s)/quiz(es) may be used.
- The penalty for cheating on an exam will be failure from the class.

Freedom in learning: Under Board of Regents and University policy student academic performance may be evaluated solely on an academic basis, not on opinions or conduct in matters unrelated to academic standards. Students should be free to take reasoned exception to the data or views offered in any course of study and to reserve judgment about matters of opinion, but they are responsible for learning the content of any course of study for which they are enrolled. Students who believe that an academic evaluation reflects prejudiced or capricious consideration of student opinions or conduct unrelated to academic standards should contact the dean of the college which offers the class to initiate a review of the evaluation.

Topics/Course Schedule: Chapters 1-8, see attached schedule (subject to revision).

Tentative Course Schedule

Class	Date(s)	Topics	Text Sections
1	1/13	**Digital Systems and Binary Numbers**	1.9
2	1/15		1.9
3	1/17		1.1-1.2
1/20		**Holiday**	
4	1/22		1.3-1.4
5	1/24		1.5-1.6
6	1/27		1.7-1.8
7	1/29	**Boolean Algebra and Logic Gates**	2.1-2.2
8	1/31		2.2-2.3
9	2/3		2.3-2.4
10	2/5		2.5-2.6
			2.7-2.9
11	2/7	**Gate-Level Minimization**	3.1-3.2
12	2/10		3.2-3.3
13	**2/12**	**Exam #1** (Chapters 1 - 2 material)	
14	2/14		3.4-3.5
2/17		**Holiday**	
15	2/19		3.6-3.7
16	2/21	**Combinational Logic**	4.1-4.2
17	2/24		4.3-4.4
18	2/26		4.5
19	2/28		4.7-4.8
20	3/3		4.9-4.10
21	3/5	**Synchronous Sequential Logic**	5.1-5.2
22	3/7		5.3
3/10 – 3/14		**Spring Break**	
23	3/17		5.3
24	3/19		5.4
25	3/21		5.5
26	3/24	**Registers and Counters**	6.1-6.2
27	3/26		6.2-6.3
28	3/28		6.4
29	3/31	**Exam #2** (Chapters 3 - 5 material)	
30	4/2		6.5
31	4/4	**Memory and Programmable Logic**	7.1-7.2
32	4/7		7.2
33	4/9		7.3
34	4/11		7.4
35	4/14		7.5
36	4/16		7.6
4/18		**Holiday**	
37	4/21	**Design at Register Transfer Level**	8.1-8.2
38	4/23		8.2
39	4/25		8.4
40	4/28		8.5
41	4/30	Exam #3 **(Chapter 6-8 material)**	
42	5/2	**Make-up/review day**	
CENG 244 Final Exam: 4 - 5:50 pm, Monday, May 5, 2014, EP252			