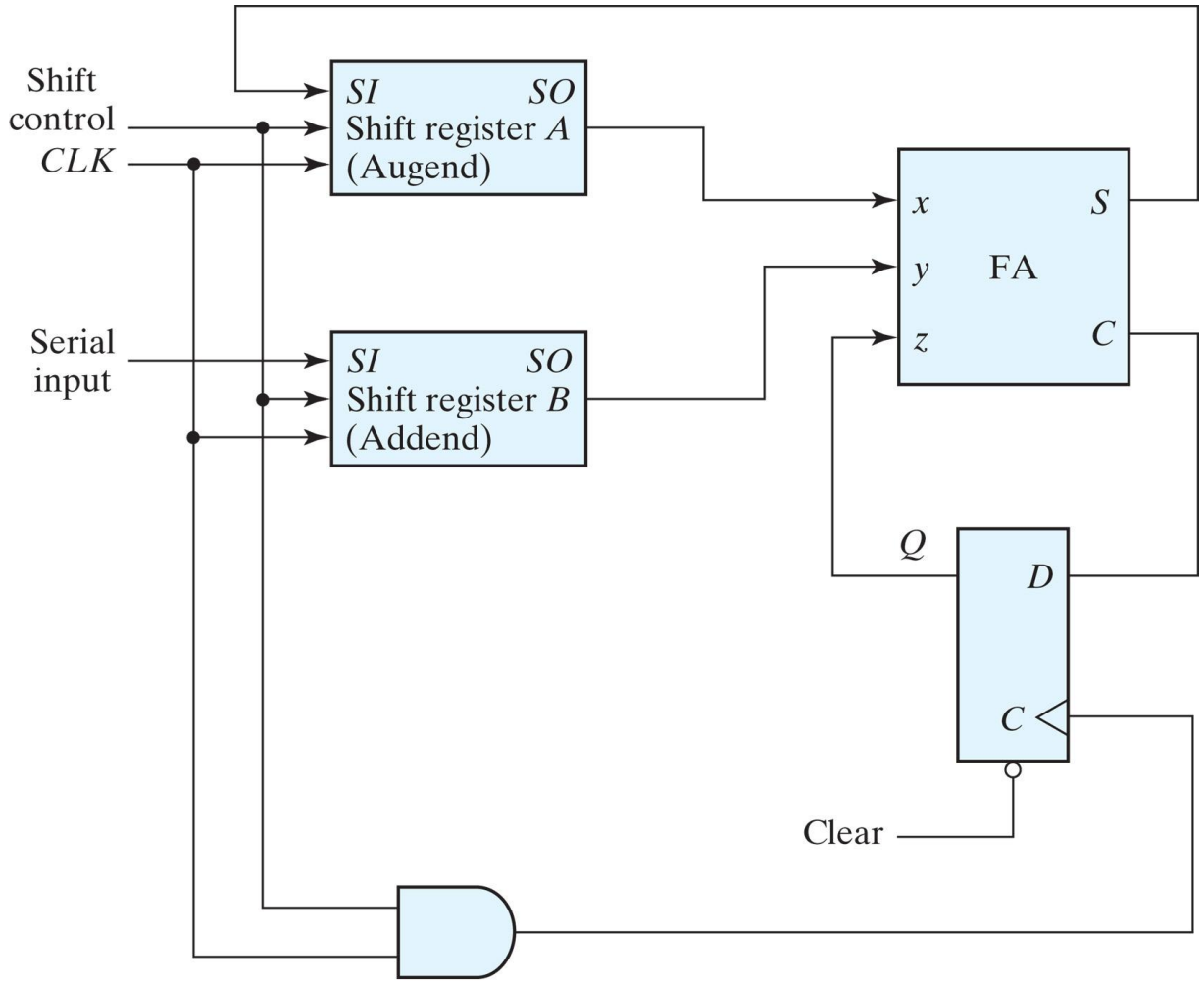
Serial adder w/ D flip-flop (Figure 6.5 of text)



What if we wished to implement this serial adder circuit using JK flip-flop?

Table 6.2
State Table for Serial Adder

Present State	Inputs		Next State	Output	Flip-Flop Inputs	
Q	x	y	Q	S	J_Q	K_Q
0	0	0	0	0	0	X
0	0	1	0	1	0	X
0	1	0	0	1	0	X
0	1	1	1	0	1	X
1	0	0	0	1	X	1
1	0	1	1	0	X	0
1	1	0	1	0	X	0
1	1	1	1	1	X	0

Get *JK* Flip-flop input equations and output (of full adder) equation :

K-Map for *S*

$Q\backslash xy$	00	01	11	10
0		$m_1 = Q'x'y$		$m_2 = Q'xy'$
1	$m_4 = Qx'y'$		$m_7 = Qxy$	

$$S = Qxy + Qx'y' + Q'x'y + Q'xy' = Q(xy + x'y') + Q'(x'y + xy') = Q(x \oplus y)' + Q'(x \oplus y)$$
$$= x \oplus y \oplus Q$$

K-Map for J_Q

$Q\backslash xy$	00	01	11	10
0			$m_3 = Q'xy$	
1	X	X	**X**	X

$$J_Q = xy$$

K-Map for K_Q

$Q\backslash xy$	00	01	11	10
0	X	X	X	X
1	$m_4 = Qx'y'$			

$$K_Q = x'y' = (x + y)'$$

Serial adder w/ *JK* flip-flop (Figure 6.6 of text)