Register Transfer Example (Figure 1.1 of text)

MEMORY UNIT

J	O	H	N

01001010 01001111 11001000 11001110   Memory Register

PROCESSOR UNIT

8 cells ← 8 cells ← 8 cells ← 8 cells   Processor Register

INPUT UNIT   Input

8 cells   Register

Keyboard   J   O   H   N   →   CONTROL
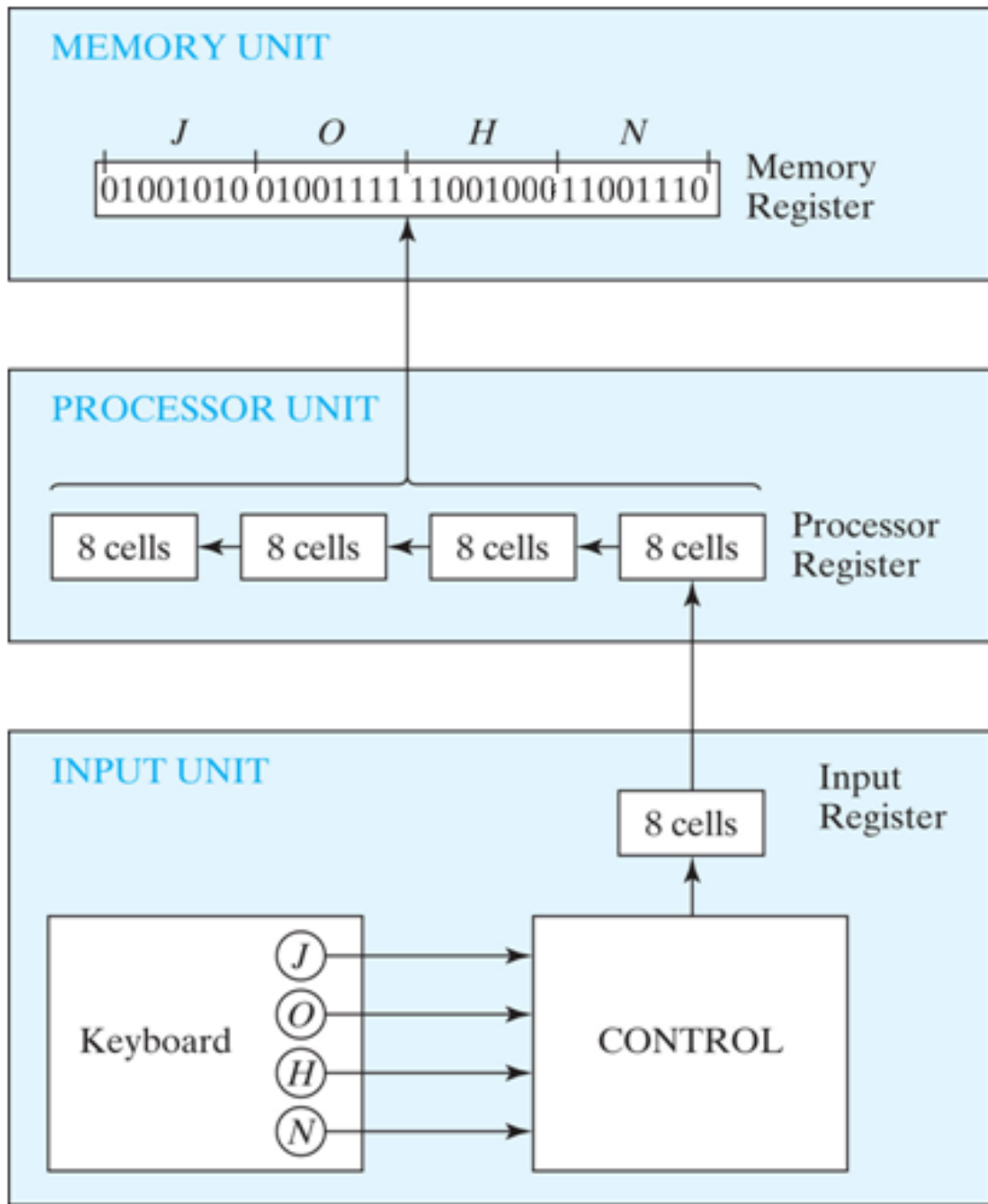
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Note: The ASCII characters have a parity bit in left position (odd 1s parity).