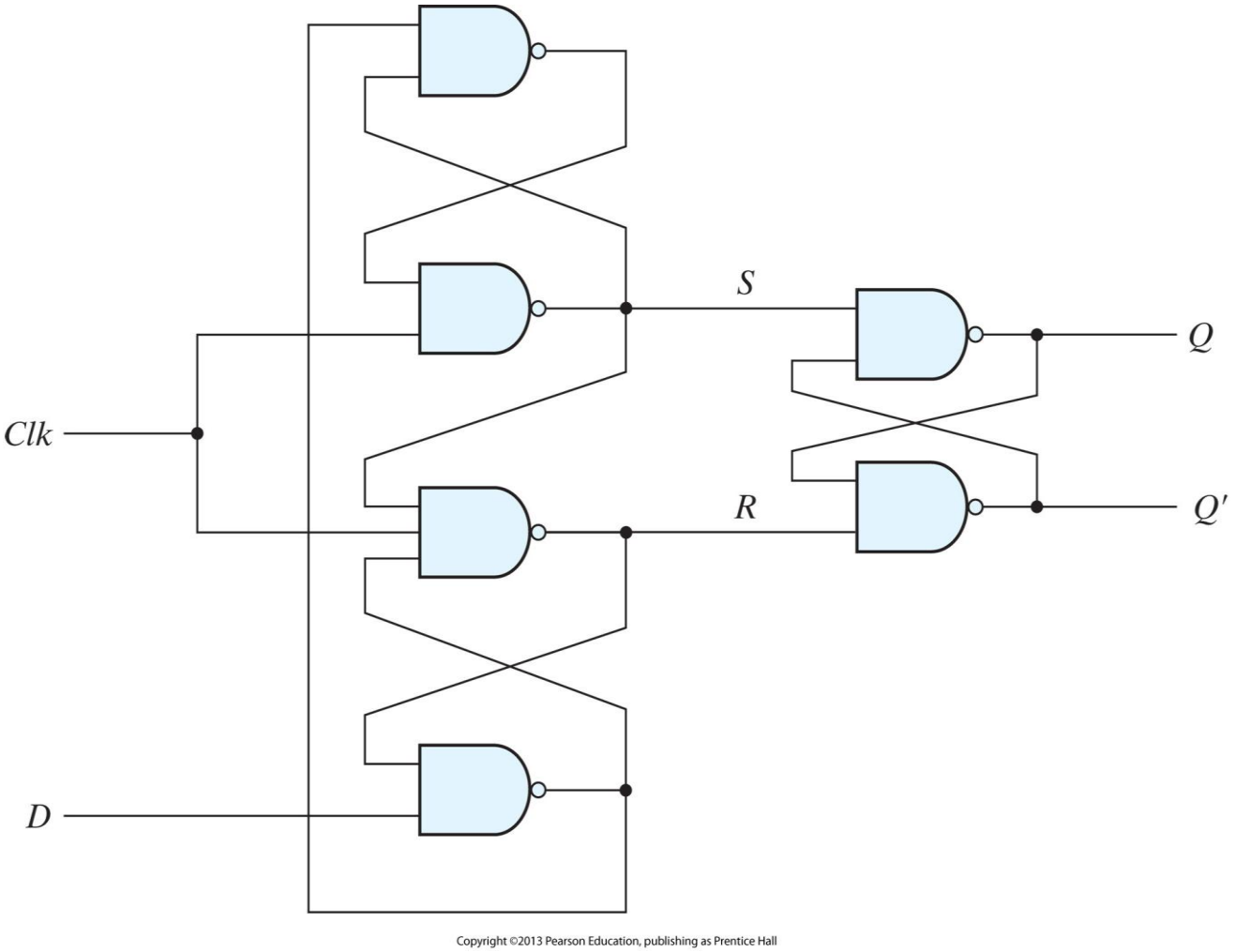
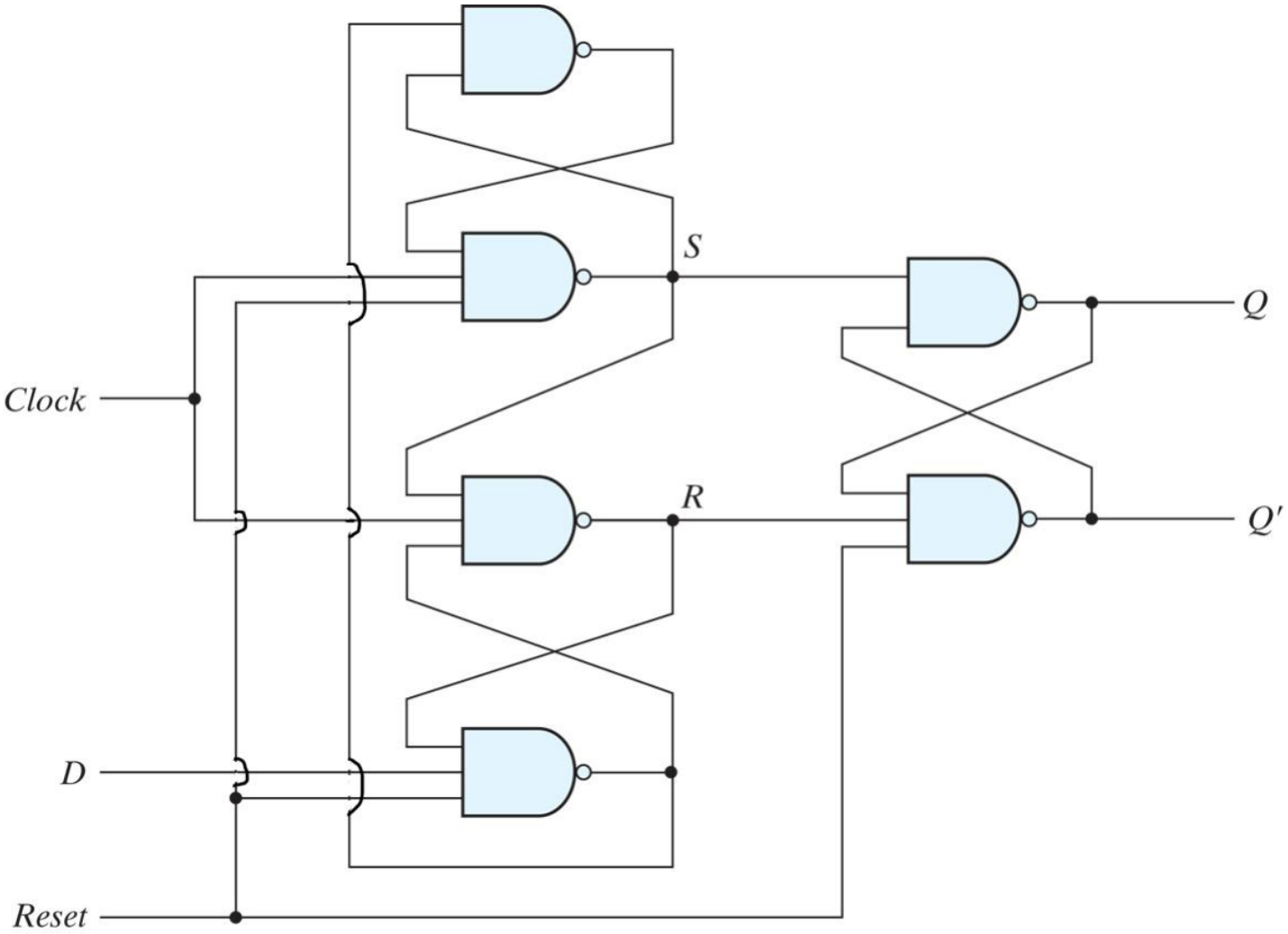
Positive-edge-triggered *D* flip-flop (Figure 5.10 of text)

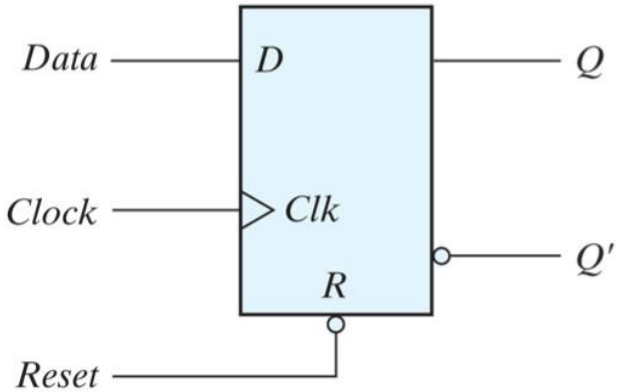


Set *S*	Reset *R*	Q	Q′	Notes
1	0	0	1	reset
1	1	0	1	no change
0	1	1	0	set
1	1	1	0	no change
0	0	1	1	‘forbidden’, don’t know next state

Positive-edge-triggered *D* flip-flop w/ asynchronous reset (Figure 5.14 of text)



(a) Circuit diagram



(b) Graphic symbol

Reset	*Clk*	*D*	*Q*	*Q'*
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0

(b) Function table