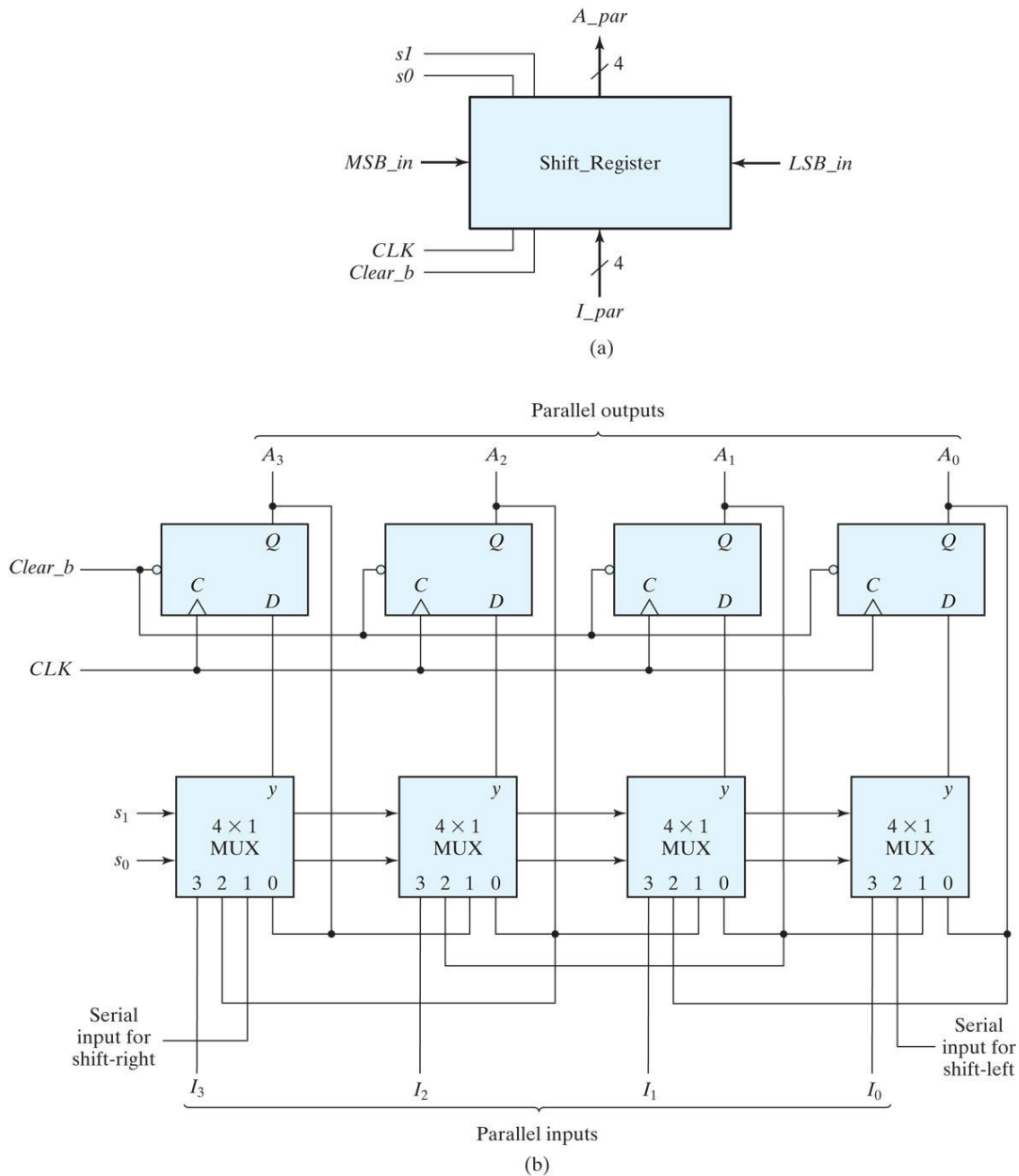


4-bit universal shift register (Figure 6.7 & Table 6.3 of text)



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Table 6.3
Function Table for the Register of Fig. 6.7

Mode Control		Register Operation
s_1	s_0	
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load